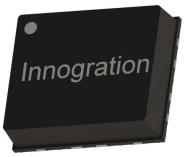
ITEV01300C9 LDMOS TRANSISTOR

Document Number: ITEV01300C9
Preliminary Datasheet V1.1

300W, 50V High Power RF LDMOS FETs

ITEV01300C9



Description

The ITEV01300C9 is a 300-watt capable, high performance, unmatched LDMOS FET, designed for wide-band commercial and industrial applications with frequencies HF to 150MHz. The device offers a more cost effective solution than traditional ceramic device，housed in 12*10mm cost effective plastic open cavity package, and heat dissipated by copper flange directly.

It is featured by single ended configuration for high power and high ruggedness, suitable for Industrial, Scientific and Medical application

- Typical performance(on Innogration test board with device soldered)

  Signal: CW , Vgs=3.2V,Vds=50V,Idq=100mA

Freq (MHz)	Pin (dBm)	Pout (dBm)	Pout (W)	Ids (A)	Gain (dB)	Eff (%)	2nd harmonic (dBc)
40.68	35	55	316	7.9	20	80	-20

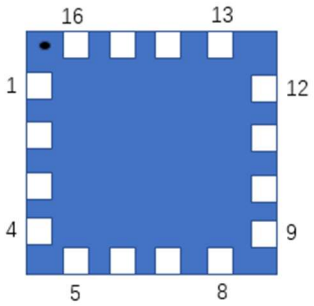
Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 136-174MHz (Commercial ground communication)
- Laser Exciter
- Synchrotron
- MRI
- Plasma generator
- Weather Radar

Pin Configuration and Description （Top view）



Pin No.	Symbol	Description
5-8	RF IN/Vgs	RF Input/Gate bias
13-16	RF OUT/Vds	RF Output/Drain bias
Others	NC	Can be left as either no use or grounding
Package Base	GND	DC/RF Ground. Proposed to be soldered to heatsink plane directly for the best CW thermal and RF performance. Soldered through vias or copper coin allowed for pulsed CW applications, but will result in excessive junction temperatures and different RF performance

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+135	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	RθJC	0.55	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (T_A = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics (per half section)					
Drain-Source Voltage V_{GS}=0, I_{DS}=1.0mA	$V_{(BR)DSS}$		135		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 75V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS(th)}$	——	2.65	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 100 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.2	——	V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 50 Vdc, I_{DQ} = 100 mA, f =100MHz, pulse width:100us, duty cycle:10%

Load 65:1 All phase angles, at 300W Pulsed CW Output Power	No Device Degradation

TYPICAL CHARACTERISTICS

Figure 1: CW Gain and Power Efficiency as a Function of Pout at 40.68MHz

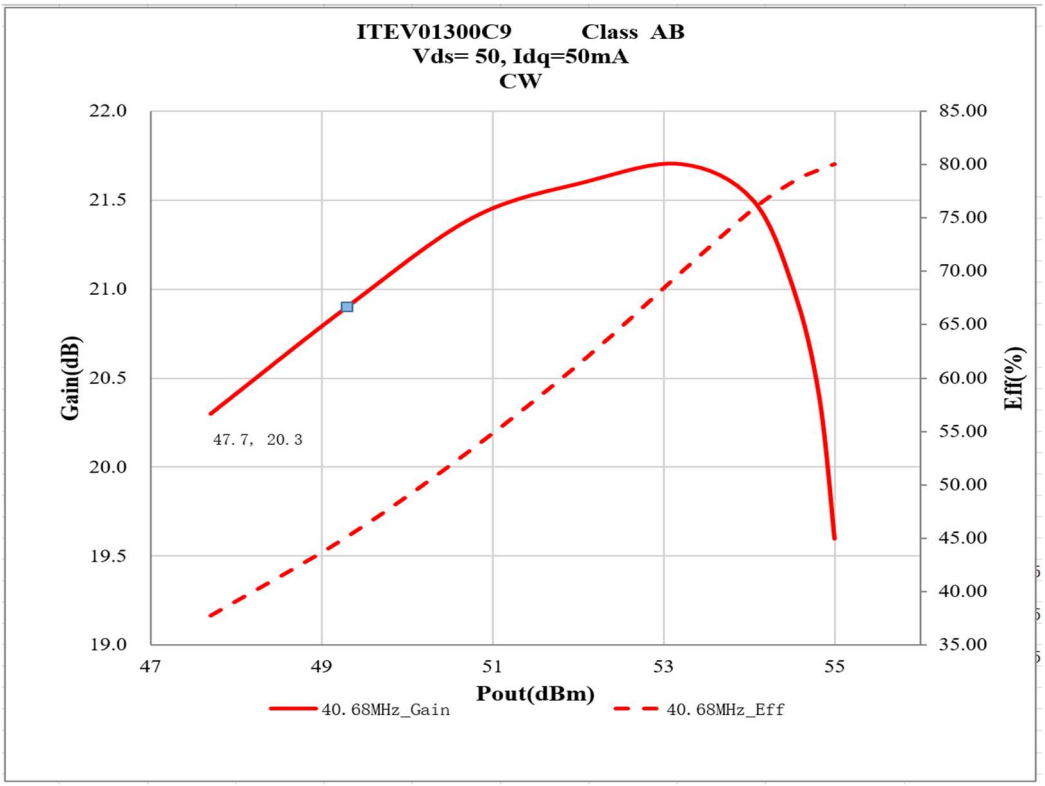
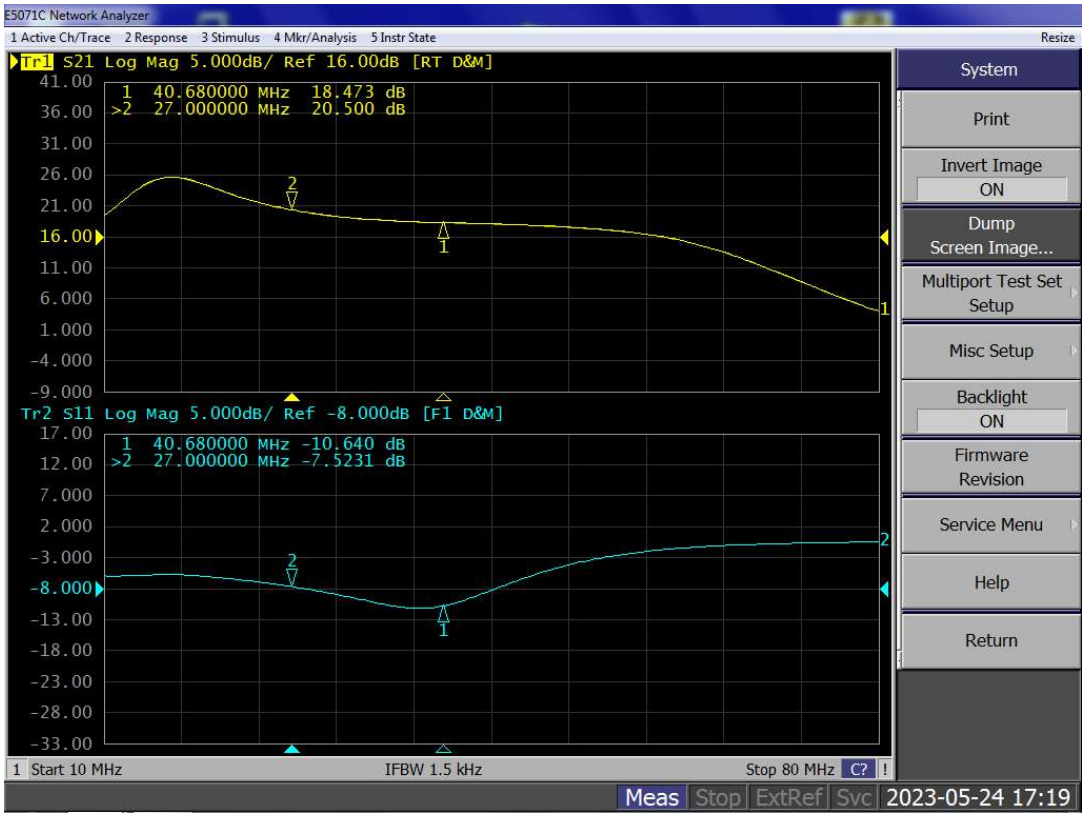


Figure 2: Network analyzer output S11/S21



Reference Circuit of Test Fixture Assembly Diagram

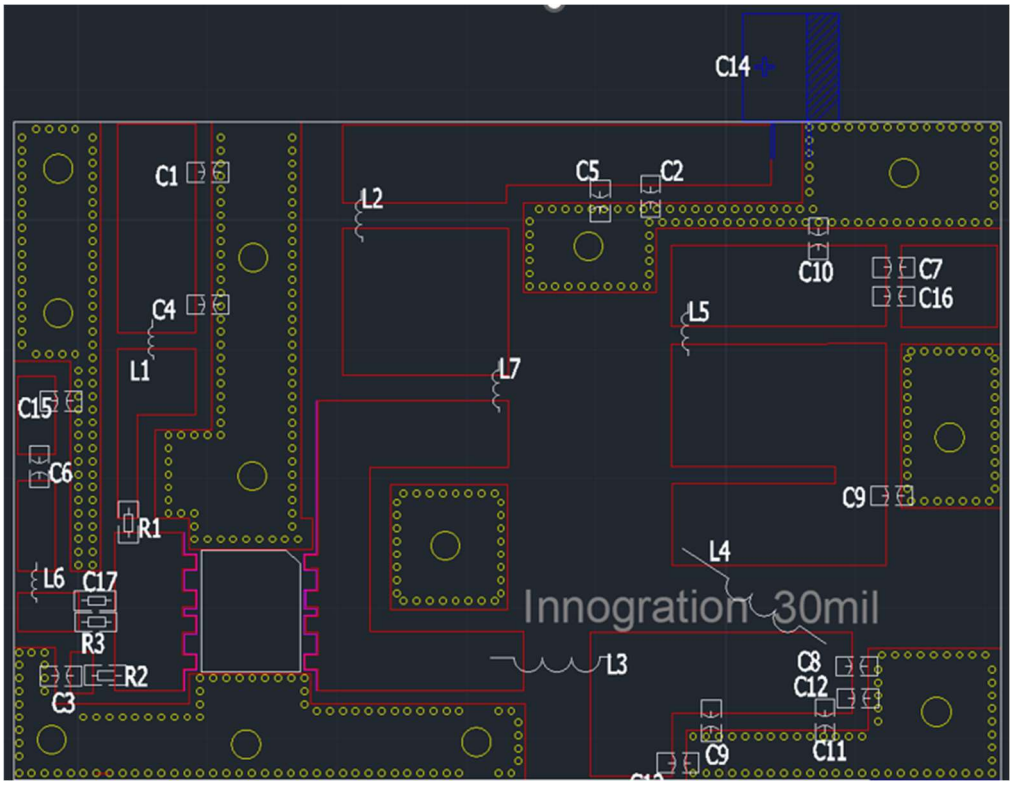
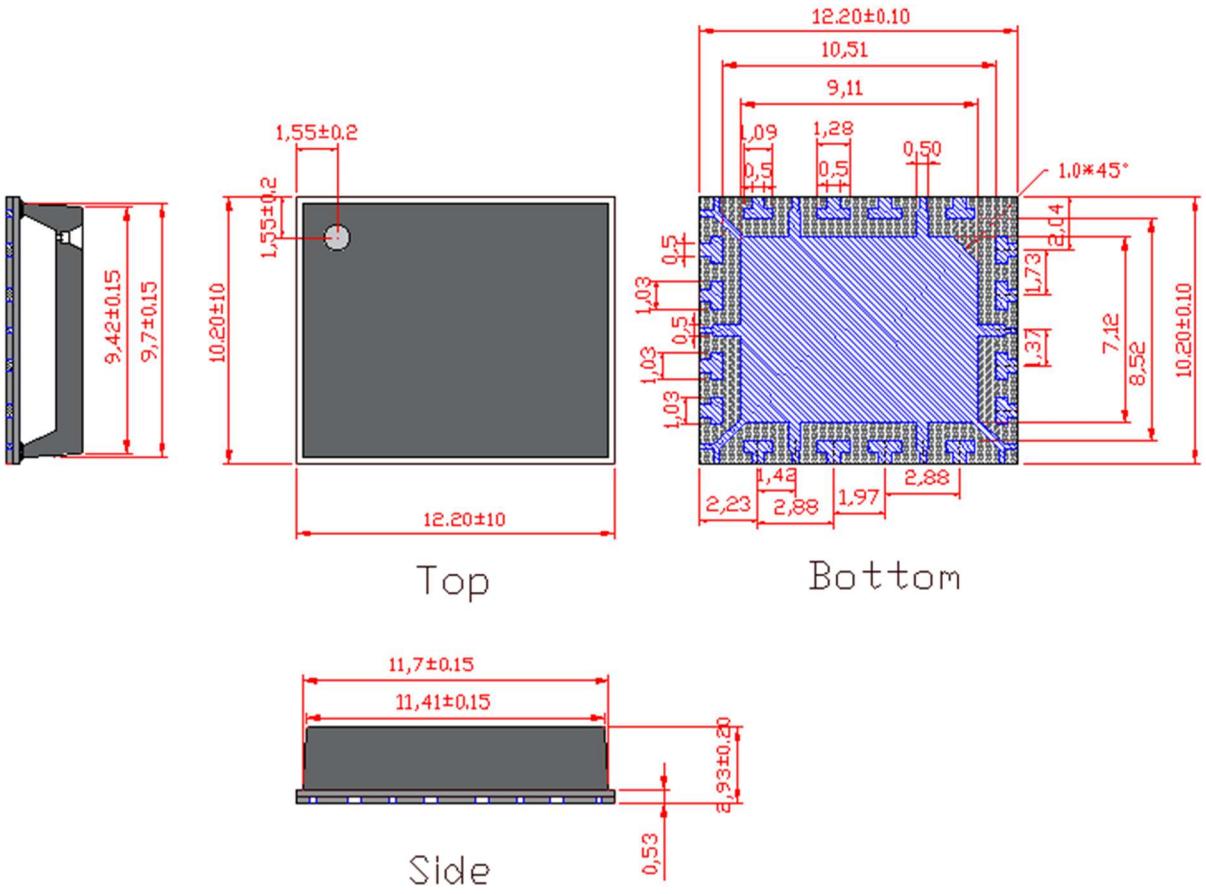


Table 5. Test Circuit Component Designations and Values

Component	Description	Suggestion
C1,C2,C3,	10uF 100V	Ceramic multilayer capacitor
C4,C5,C6,C7,C16	10nF 100V	Ceramic multilayer capacitor
C14	470uF,63V	Electrolytic Capacitor
C15	200pF	MQ101111
C8	100pF	MQ101111
C9,C11	33pF	MQ101111
C10	22pF	MQ101111
C12	150pF	MQ101111
C13	56pF	MQ101111
C15	39pF	MQ101111
L1	47nH	
L6	150nH	
R1	300Ω，1206	Chip Resistor
R2	5Ω	Chip Resistor
L2,L7	1.5mm，6 turns，Φ5	
L3	1.5mm，2 turns，Φ5	
L4	1.5mm，4 turns，Φ5	
PCB	30Mil Rogers4350	

Package Dimensions （Unit:mm）



Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2023/5/25	Rev 1.0	Preliminary Datasheet Creation
2023/8/17	Rev 1.1	Modification of package drawing on last page

Application data based on SYX-23-21

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