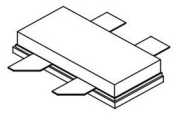
GaN HEMT 50V, 500W,2.3-2.4GHz RF Power Transistor

STBV24500BY4



Description

The STBV24500BY4 is a dual path 500watt , Input matched GaN HEMT, ideal for applications from 2.3 to 2.4GHz especially for LTE/5G. In typical 8.5-9.5dB back off condition, it can deliver 55 to 70W linearizable average power

There is no guarantee of performance when this part is used outside of stated frequencies.

- Typical RF performance on asymmetrical Doherty with device soldered

VDS= 50V, IDQ=250mA(Vgm=-3.2V，Vgp=-5.40V)

WCDMA 1 carrier performance

Freq (MHz)	Pout (dBm)	ACPR (dBc)	Gain (dB)	Efficiency (%)
2300	47.5	-30.9	15.2	54.9
2350	47.5	-30.7	15.0	54.8
2400	47.5	-30.2	14.4	54.3

Recommended driver: Class AB (1 stage discrete solution): STAV38041C6

Applications

- Asymmetrical Doherty amplifier within 2.3-2.4GHz
- S band power amplifier
- CW or pulsed Amplifier

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically –5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically –5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Figure 1: Pin Connection definition

Transparent top view (Backside grounding for source)

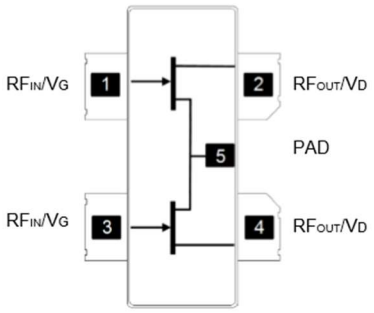


Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	55	Vdc

Maximum gate current	Igs	65	mA
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA T_C= 85°C, at Pd=50W, on Doherty application board	$R_{\theta JC}$	1	°C /W

Table 3. Electrical Characteristics (TA = 25℃ unless otherwise noted)

DC Characteristics (Main path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=25.2mA	V_{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 25.2mA	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	VDS =50V, IDS=150mA, Measured in Functional Test	$V_{GS(Q)}$		-3.07		V

DC Characteristics (Peak path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=39.6mA	V_{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 39.6mA	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	VDS =50V, IDS=150mA, Measured in Functional Test	$V_{GS(Q)}$		-3.0		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	2.35GHz, Pout=55W WCDMA 1 Carrier in Doherty circuit All phase, No device damages	VSWR		10:1		

Figure 2: Median Lifetime vs. Channel Temperature

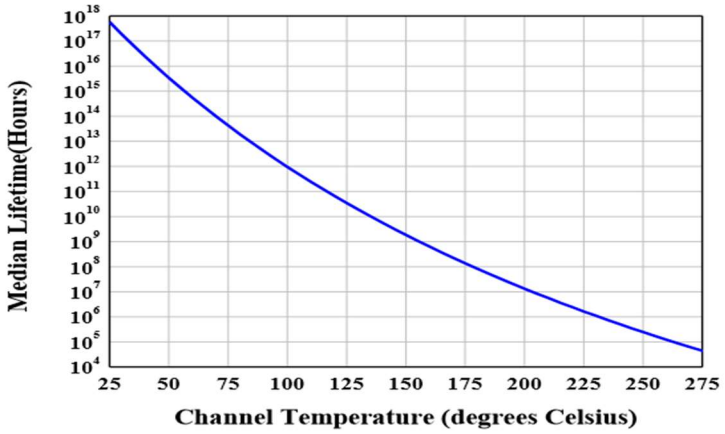
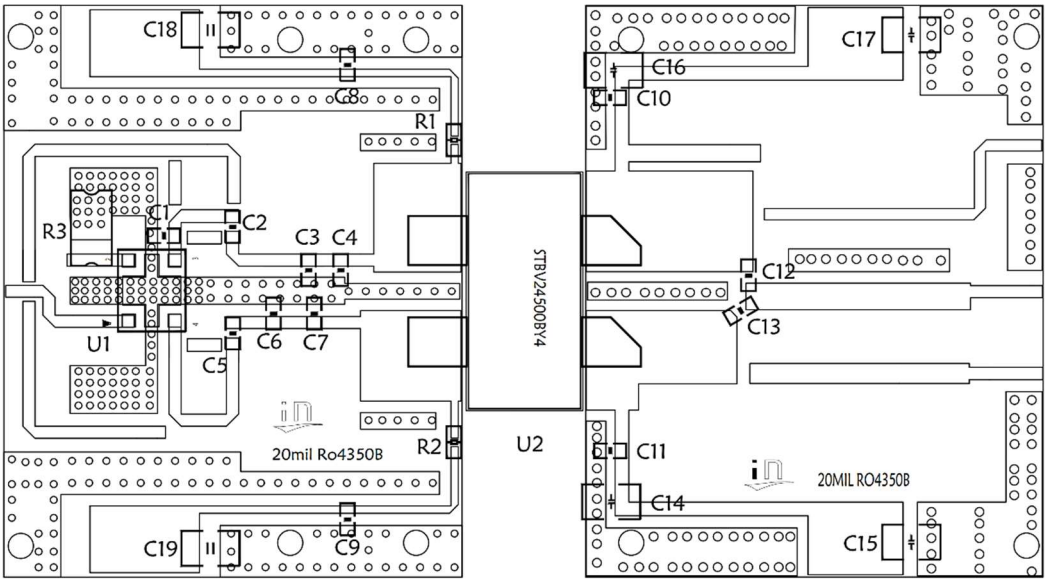
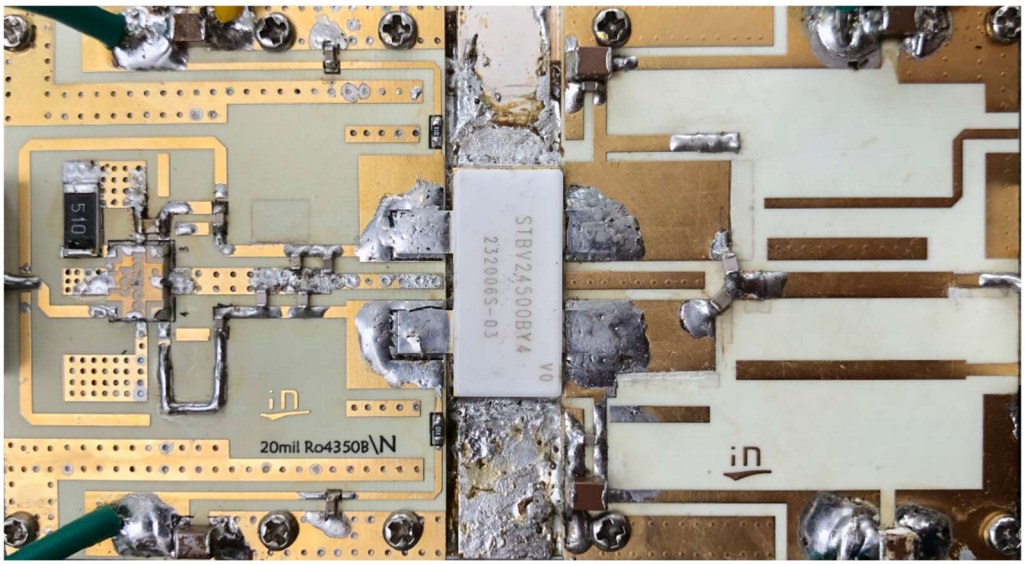


Figure 3: Picture of application board Doherty circuit for 2.3-2.4GHz





Reference	Footprint	Value	Quantity
C1	0603	0.4pF/250V	1
C2, C13	0603	10pF/250V	2
C3	0603	2.0pF/250V	1
C4, C6, C7	0603	1.1pF/250V	3
C5, C8, C9, C10, C11	0603	20pF/250V	5
C12	0603	1.8pF/250V	1
C14, C15, C16, C17, C18, C19	1210	10uF/100V	6
R1, R2	0603	10R	2
R3	2512	51R	1
U1	6.35*5.08mm	HC2500P03	1
U2	BY4	STBV24500BY4	1

Figure 3: Efficiency and power gain as function of Pout

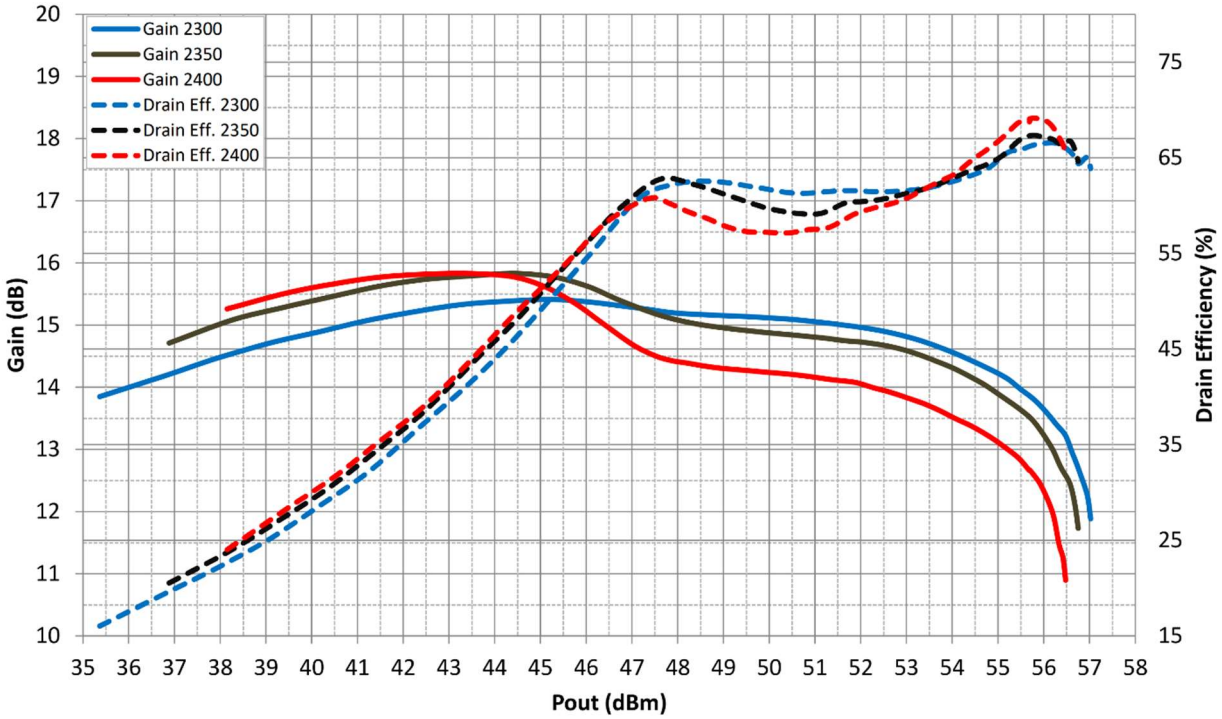
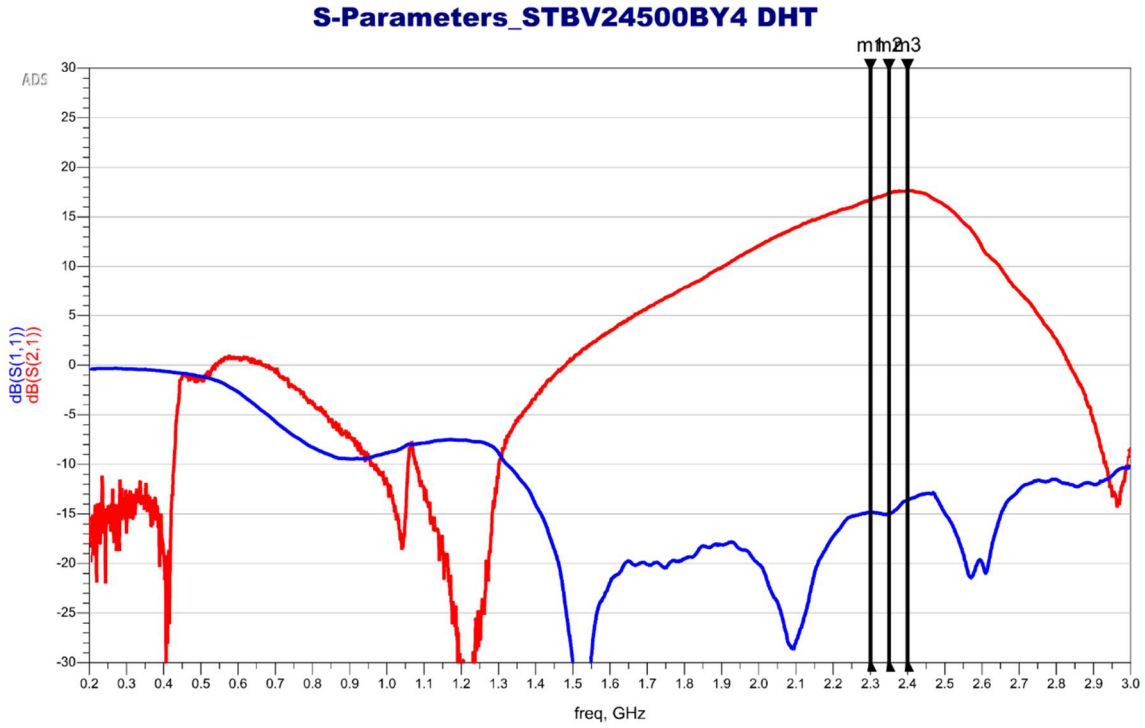
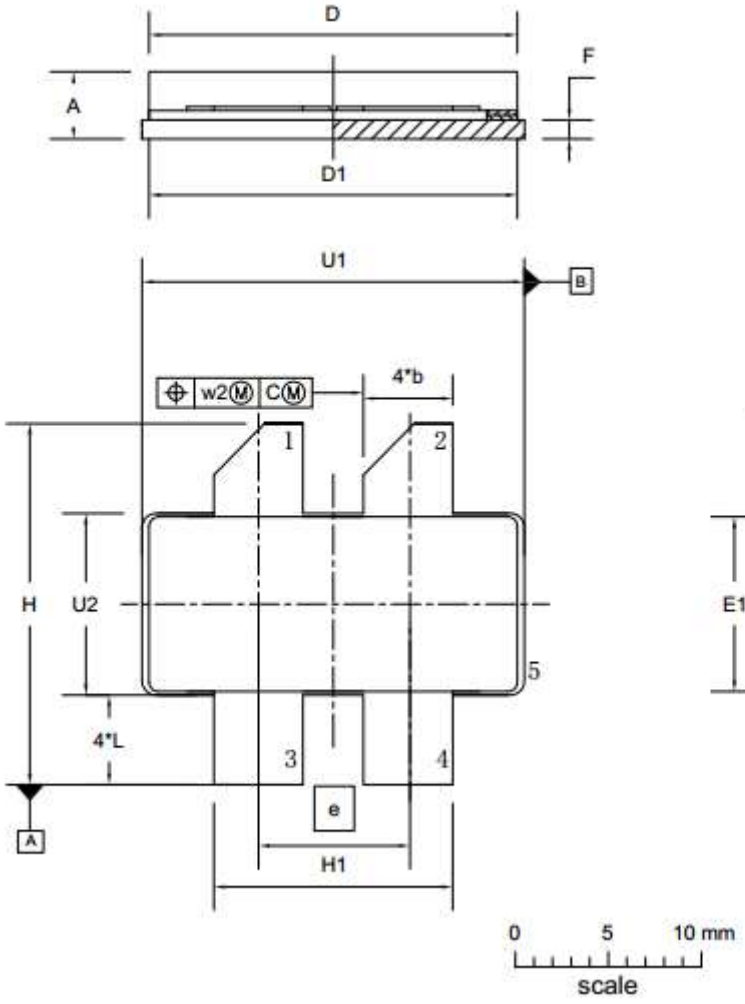


Figure 5: Network analyzer output, S11 and S21

m1 freq=2.300 GHz dB(S(2,1))=16.737 dB(S(1,1))=-14.838	m2 freq=2.350 GHz dB(S(2,1))=17.363 dB(S(1,1))=-14.992	m3 freq=2.400 GHz dB(S(2,1))=17.602 dB(S(1,1))=-13.611



Earless Flanged Ceramic Package; 4 leads



Drain		Gate		Source
1	2	3	4	5

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H1	L	Q	U_1	U_2	W_1	W_2
mm	4.72 3.43	4.67 4.93	0.15 0.08	20.02 19.61	19.96 19.66	7.90	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	12.98 12.73	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.194 0.184	0.006 0.003	0.788 0.772	0.786 0.774	0.311	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.511 0.501	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B4					03/12/2013

Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2023/5/16	**V1.0**	**Objective Datasheet Creation**
2023/5/30	**V1.0**	**Preliminary Datasheet Creation**

Notice