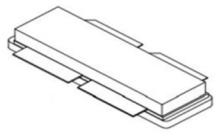
GaN 50V,800W, RF Power Transistor

SQ1280RVPS



Description

The SQ1280RVPS is a push pull 800W capable, internally matched GaN HEMT, ideal for multiple applications from 0.96 to 1.4GHz. It is optimized thermally to support higher duty cycle or longer pulse up to CW application.

In typical wideband application from 960 to 1215MHz, it can deliver >600W across the full band.

There is no guarantee of performance when this part is used outside of stated frequencies.

- Typical Pulsed CW performance at 960-1215MHz applications

SQ1280RVPS^{V1} Vgs=-3.26V Vds=50V Idq=50mA, Pulse 12us 50%								
Freq (MHz)	Psat (dBm)	Psat (W)	IDS (A)	Pin (dBm)	Gain (dB)	Eff (%)	2nd (dBc)	3rd (dBc）
960	58.63	729.5	13.91	45.63	13.00	52.44	-26.2	-26.0
1000	58.20	660.7	12.91	45.70	12.50	51.18	-38.9	-26.3
1050	58.78	755.1	13.78	45.56	13.22	54.80	-28.5	-42.4
1100	58.69	739.6	12.83	45.42	13.27	57.65	-29.3	-42.2
1150	58.23	665.3	12.71	45.11	13.12	52.34	-26.5	-42.0
1200	57.92	619.4	11.56	45.52	12.40	53.58	-22.5	-42.2
1215	58.45	699.8	12.46	45.24	13.21	56.17	-21.0	-42.0

Applications

- L band power amplifier
- Avionics datalink

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically –5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically –5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc

Gate--Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum gate current	Igs	100	mA
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA T_C= 25°C, at Pout=600W @1215MHz	$R_{\theta JC}$	0.22	°C /W

Table 3. Electrical Characteristics (TA = 25℃ unless otherwise noted)

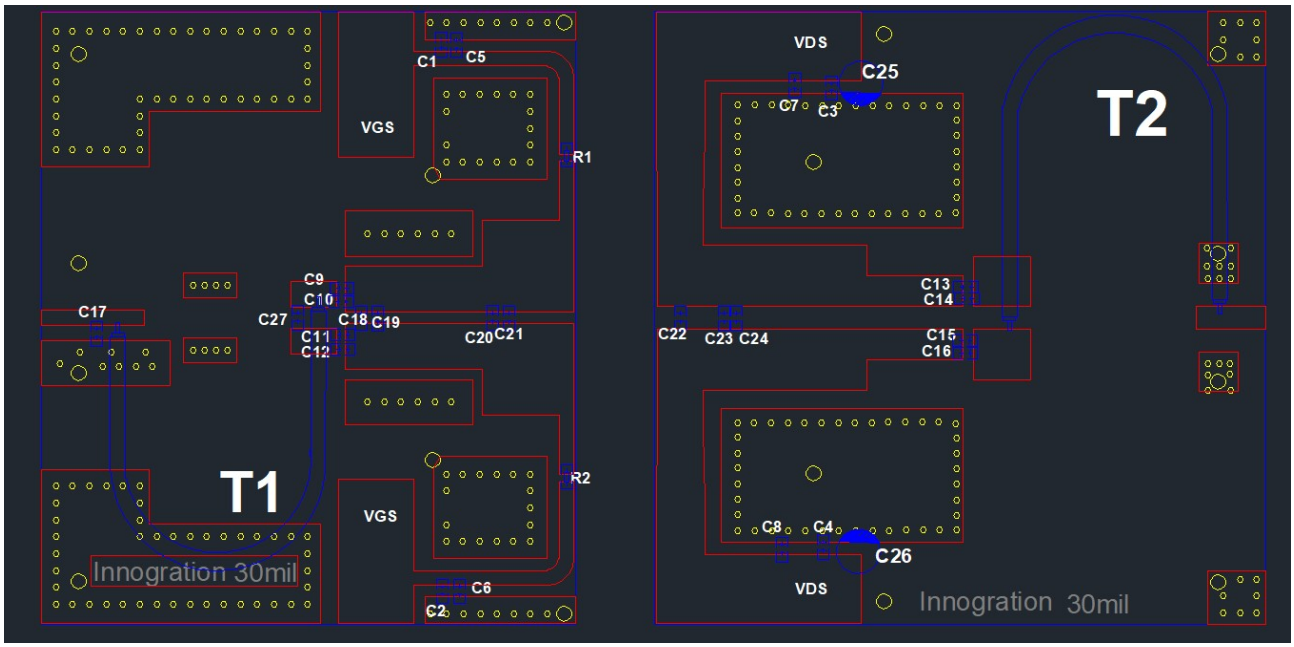
DC Characteristics (Each path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=100mA	V_{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 100mA	$V_{GS(th)}$	-4	-	-2	V
Gate Quiescent Voltage	VDS =50V, IDS=180mA, Measured in Functional Test	$V_{GS(Q)}$		--3.2		V

Ruggedness Characteristics

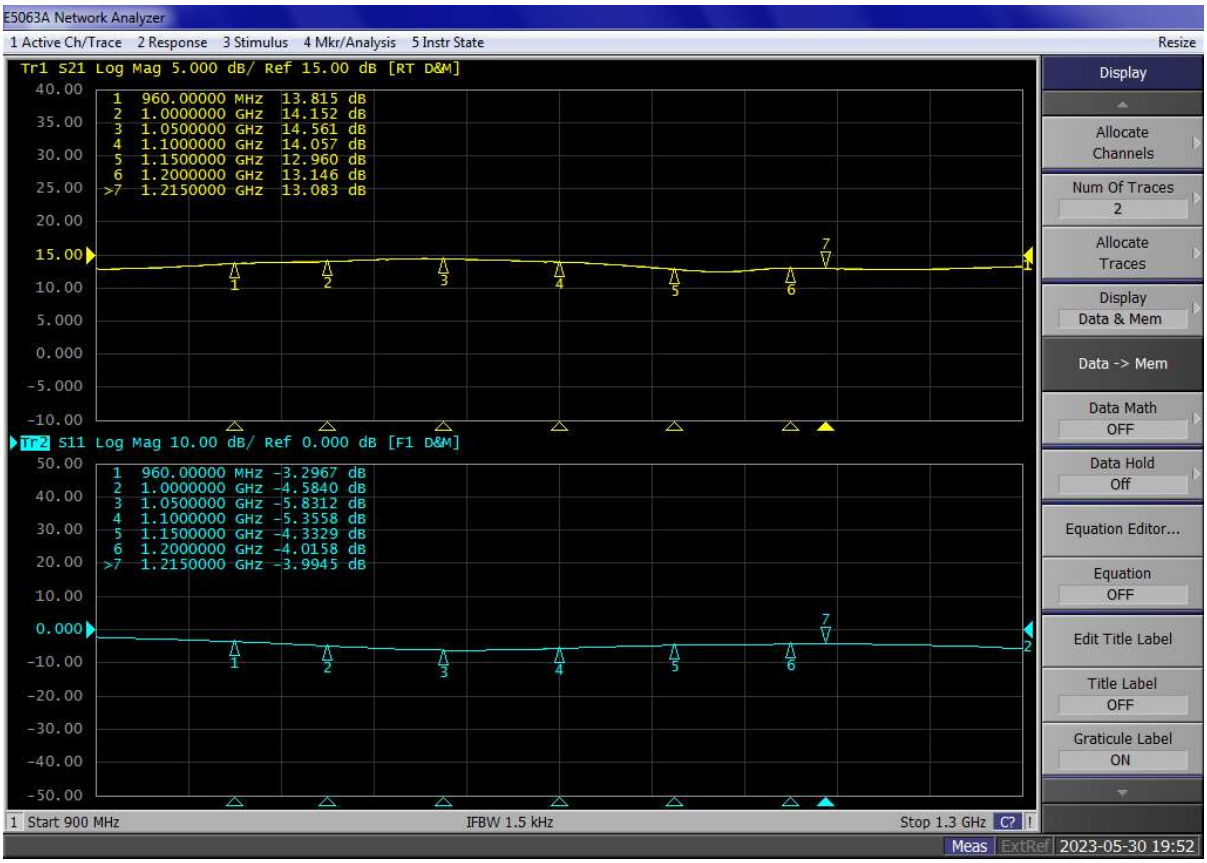
Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	1215MHz, Pout=600W pulse CW All phase, No device damages	VSWR		5:1		

Figure 1: Reference design circuit (PCB DWG file upon request)



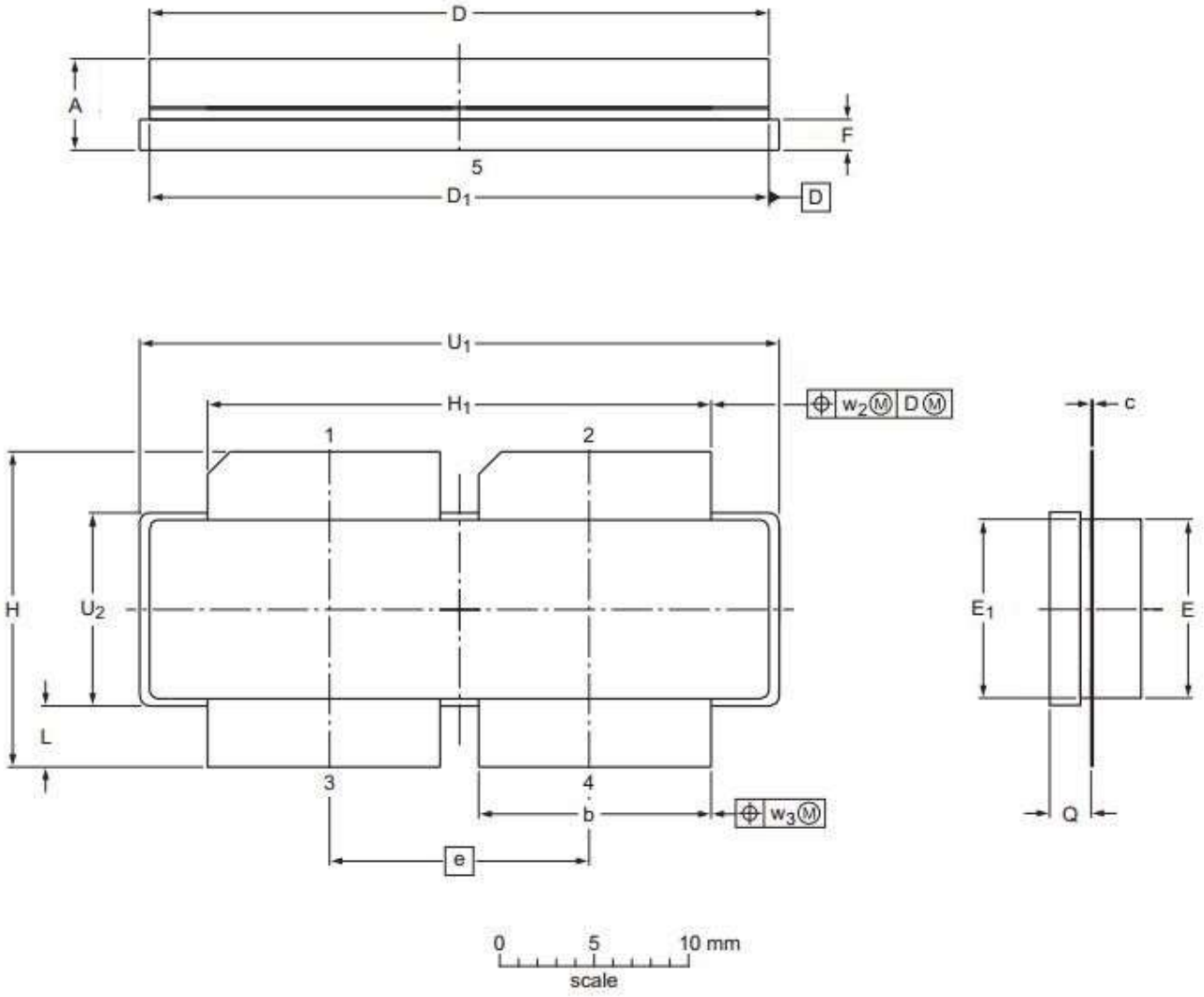
Component	Description	Suggestion
C1,C2,C3,C4	10uF	10uF/100V
C5,C6,C9,C10,C11,C12	39pF	MQ101111
C7,C8	100pF	MQ101111
C13,C14,C15,C16	18pF	MQ101111
C17	1pF	MQ101111
C18,C22,C21	1.5pF	MQ101111
C19	3.9pF	MQ101111
C20	6.2pF	MQ101111
C23	3pF	MQ101111
C24	0.5pF	MQ101111
C25,C26	4700uF/50V	Electrolytic Capacitor
C27	2pF	MQ101111
R1,R2	10 Ω	Chip Resistor
T1	25 ohm,60mm	RFSFBU-086-25
T2	50 ohm ,70mm	SFF-35-3
PCB	30Mil RF-35TC-A	

Figure 2: Network analyzer output S11/S21



Package Outline

Earless flanged ceramic package; 4 leads（1、2—DRAIN、3、4—GATE、5—SOURCE）



UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	Q	U_1	U_2	W_2	W_2
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	2.26 2.01	32.39 32.13	10.29 10.03	0.25	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.089 0.079	1.275 1.265	0.405 0.395	0.01	0.01

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4					03/12/2013

Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2023/5/31	**V1.0**	**Preliminary Datasheet Creation**

Application data based on:TC-23-33

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