



## GaN 50V,480W, RF Power Transistor

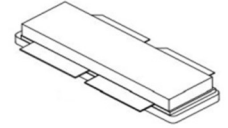
### SQ3048RVPS

#### Description

The SQ3048RVPS is a push pull 480W capable, internally matched GaN HEMT, ideal for multiple applications up to 3GHz. It is optimized thermally to support higher duty cycle or longer pulse up to CW application.

In typical wideband application from 700 to 910MHz, it can deliver >400W across the full band.

There is no guarantee of performance when this part is used outside of stated frequencies.



- Typical Pulsed CW performance at 700-910MHz applications

SQ3048RVPS <sup>V0</sup> V <sub>DS</sub> =50V V <sub>GS</sub> =-3.29V I <sub>DQ</sub> =180mA Pulse Width 20us 50%								
Freq (MHz)	Psat (dBm)	Psat (W)	IDS (A)	Pin (dBm)	Gain (dB)	Eff(%)	2 <sup>nd</sup> Harmonic(dBc)	3 <sup>rd</sup> Harmonic(dBc)
700	57.04	505.8	8.4	36.98	20.06	60	-18.5	-43.4
750	56.6	457.1	7.4	36.9	19.7	62	-21.7	-39.2
800	56.34	430.5	7.1	36.28	20.06	60	-24.7	-34.8
850	56.87	486.4	7.9	36.03	20.84	62	-24.5	-45.2
900	56.56	452.9	8.0	36.02	20.54	57	-30.7	-38.9
910	56.39	435.5	7.8	35.69	20.7	56	-34.2	-36.4

#### ● Applications

- P band power amplifier
- UHF TV
- Public Safety Radio
- Data link power amplifier

#### Important Note: Proper Biasing Sequence for GaN HEMT Transistors

##### Turning the device ON

1. Set VGS to the pinch-off (VP) voltage, typically -5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

##### Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically -5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V <sub>DSS</sub>	+200	Vdc
Gate--Source Voltage	V <sub>GS</sub>	-8 to +0.5	Vdc



Operating Voltage	$V_{DD}$	55	Vdc
Maximum gate current	$I_{gs}$	60	mA
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature	$T_c$	+150	°C
Operating Junction Temperature	$T_j$	+225	°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA $T_c = 25^\circ\text{C}$ , at $P_{out} = 400\text{W}$ @900MHz	$R_{\theta JC}$	0.31	°C /W

**Table 3. Electrical Characteristics ( $T_A = 25^\circ\text{C}$  unless otherwise noted)**

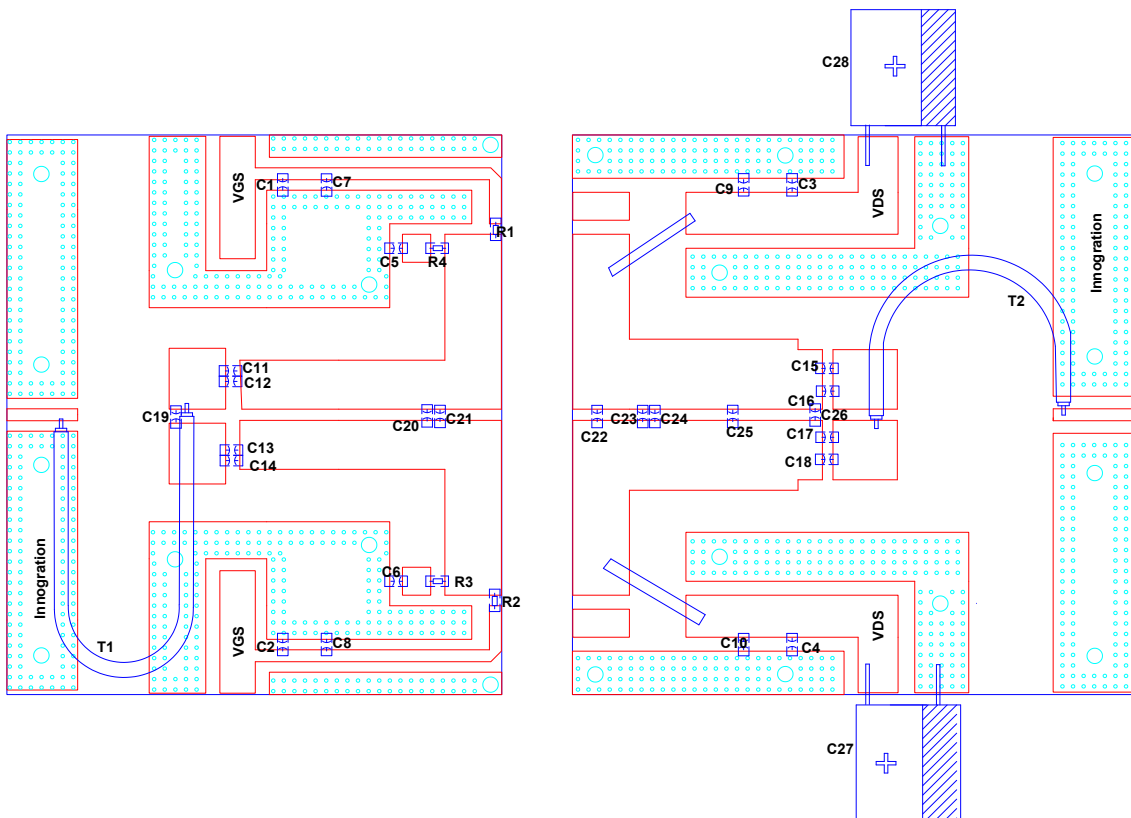
DC Characteristics (Each path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = -8\text{V}$ ; $I_{DS} = 60\text{mA}$	$V_{DSS}$		200		V
Gate Threshold Voltage	$V_{DS} = 10\text{V}$ , $I_D = 60\text{mA}$	$V_{GS(th)}$	-4	-	-2	V
Gate Quiescent Voltage	$V_{DS} = 50\text{V}$ , $I_{DS} = 180\text{mA}$ , Measured in Functional Test	$V_{GS(Q)}$		-3.2		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	900MHz, $P_{out} = 400\text{W}$ pulse CW All phase, No device damages	VSWR		5:1		

**Figure 1: Reference design circuit (PCB DWG file upon request)**





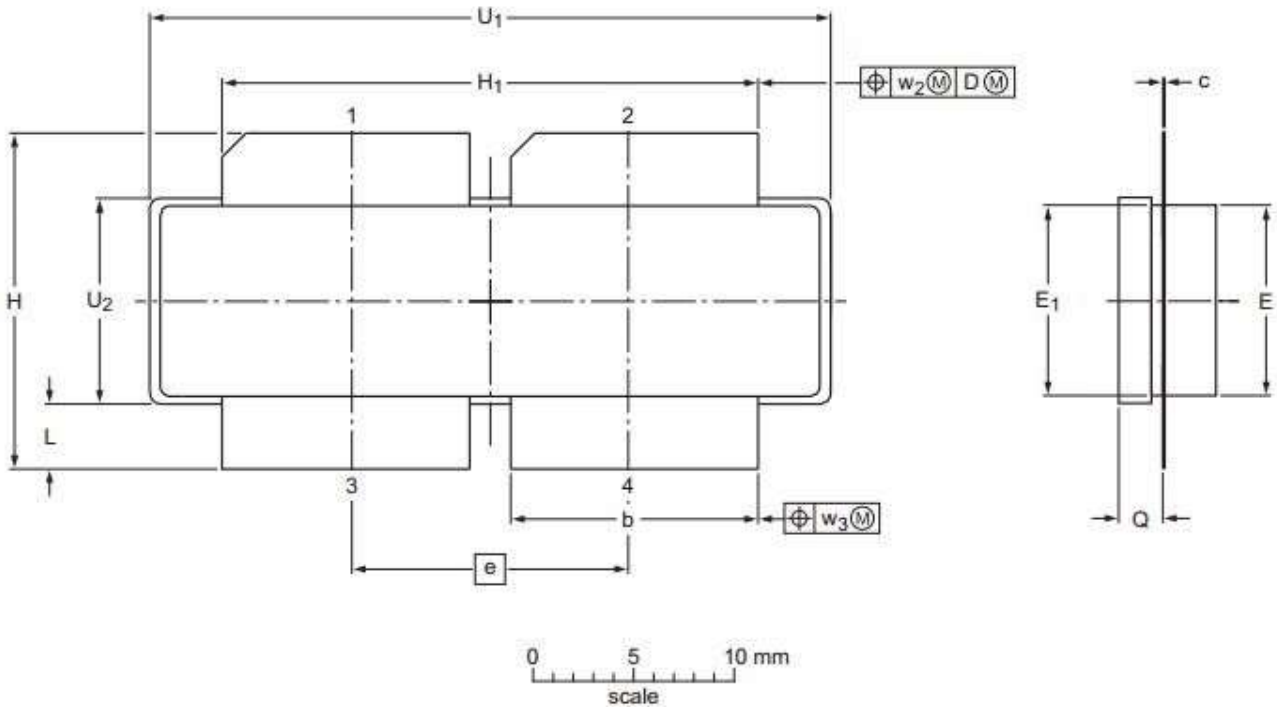
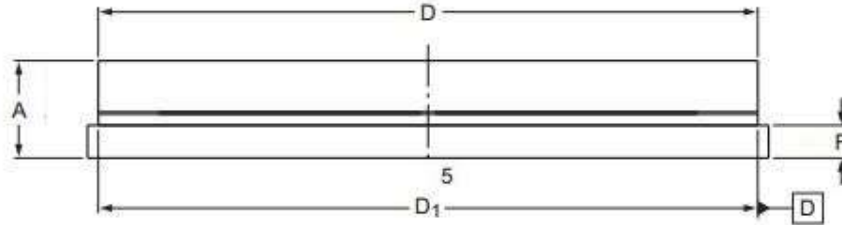
Component	Description	Suggestion
C1~C6	10uF	10uF/100V
C7~C10	200pF	MQ101111
C11~C14	27pF	MQ101111
C15~C18	18pF	MQ101111
C19	3pF	MQ101111
C20	12pF	MQ101111
C21,C24	6.8pF	MQ101111
C22	5.1pF	MQ101111
C23	3.9pF	MQ101111
C25	6.2pF	MQ101111
C26	3.3pF	MQ301111
C27,C28	4700uF/63V	Electrolytic Capacitor
R1,R2	51 Ω	Chip Resistor
R2,R3	10 Ω	Chip Resistor
T1	50ohm,45mm	RFSFBU-086-50
T2	25 Ohm ,55mm	SFF-25-1.5
PCB	Rogers 4350B	30mils





## Package Outline

Earless flanged ceramic package; 4 leads (1、2—DRAIN、3、4—GATE、5—SOURCE)



UNIT	A	b	c	D	D <sub>1</sub>	e	E	E <sub>1</sub>	F	H	H <sub>1</sub>	L	Q	U <sub>1</sub>	U <sub>2</sub>	W <sub>2</sub>	W <sub>2</sub>
mm	4.7	11.81	0.18	31.55	31.52	13.72	9.50	9.53	1.75	17.12	25.53	3.48	2.26	32.39	10.29	0.25	0.25
	4.2	11.56	0.10	30.94	30.96		9.30	9.27	1.50	16.10	25.27	2.97	2.01	32.13	10.03		
inches	0.185	0.465	0.007	1.242	1.241	0.540	0.374	0.375	0.069	0.674	1.005	0.137	0.089	1.275	0.405	0.01	0.01
	0.165	0.455	0.004	1.218	1.219		0.366	0.365	0.059	0.634	0.995	0.117	0.079	1.265	0.395		

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4					03/12/2013



## Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2023/5/5	V1.0	Preliminary Datasheet Creation

Application data based on: HL-23-15

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