SK1685V GaN TRANSISTOR

Document Number: SK1685V
Preliminary Datasheet V1.1

Gallium Nitride 50V, 800W, RF Power Transistor

SK1685VS

SK1685V

Description

The SK1685V is a 800-watt, internally matched GaN HEMT, designed for pulsed amplifier applications with frequencies from 1.2-1.6GHz.

There is no guarantee of performance when this part is used in applications designed outside of these frequencies.

It is recommended to use this device only at pulse condition, and power rating will decrease according to longer pulse width and higher duty cycle

- Typical **pulse** Performance (On Innogration **1.2-1.4GHz** fixture with device soldered):

V_{DD} = 50 Volts, I_{DQ} = 50 mA, Pulse CW, Pulse width=100us, Duty cycle=10%.

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P4dB (dBm)	P4dB (W)	P4dB Eff(%)
1200	58.48	705.3	62.8	19.71	59.29	850.0	67.1
1250	58.24	667.5	58.7	19.93	59.3	851.0	63.2
1300	58.33	680.1	57.1	19.92	59.4	871.1	61.1
1350	58.52	711.3	58.3	19.8	59.42	874.5	61.0
1400	58.39	690.4	57.8	19.65	59.31	852.2	62.3

- Typical **pulse** Performance (On Innogration **1.2-1.6GHz** fixture with device soldered):

V_{DD} = 50 Volts, I_{DQ} = 50 mA, Pulse CW, Pulse width=100us, Duty cycle=10%.

Freq(MHz)	Pin(dBm)	Psat(dBm)	Psat(W)	Ids(A)	Gain(dB)	Eff(%)
1200	42.62	58.72	744.7	2.62	16.1	56.8
1300	42.73	58.71	743.0	2.78	16.0	53.5
1400	42.67	59.09	811.0	3.05	16.4	53.2
1500	42.8	58.71	743.0	2.86	15.9	52.0
1600	43.12	59.26	843.3	2.29	16.1	73.7

Applications and Features

- Suitable for broad band application in L band
- Thermally Enhanced Industry Standard Package
- High Reliability Metallization Process
- Excellent thermal Stability and Excellent Ruggedness
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

■ **Turning the device ON**

1) Set VGS to the pinch--off (VP) voltage, typically –5 V
2) Turn on VDS to nominal supply voltage (50 V)
3) Increase VGS until IDS current is attained
4) Apply RF input power to desired level

■ **Turning the device OFF**

1) Turn RF power off
2) Reduce VGS down to VP, typically –5 V
3) Reduce VDS down to 0 V
4) Turn off VGS

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0	Vdc
Operating Voltage	V_{DD}	0 to 55	Vdc
Maximum Forward Gate Current @ T_C = 25°C	Igmax	120	mA
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case,P_{OUT}=800W @1.4GHz 20us/10%, Tcase=85°C, 50 Vdc, I_{DQ} =50 mA	$R_{\theta JC}$	0.2	°C/W

Table 3. Electrical Characteristics (TA = 25℃ unless otherwise noted)

DC Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{GS}=-8V; I_{DS}=120mA	V_{DSS}	——	200	——	V
Gate Threshold Voltage	V_{DS} = 10V, I_D = 120mA	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	V_{DS} =50V, I_{DS}=50mA, Measured in Functional Test	$V_{GS(Q)}$	——	-3.3	——	V

Functional Tests (In Innogration Test Fixture, 50 ohm system) :V_{DD} = 50Vdc, I_{DQ} =100 mA, f = 1400MHz, Pulse CW, Pulse width=40us, Duty cycle=20%.

Characteristic	Symbol	Min	Typ	Max	Unit
Power Gain @ $P_{\_1dB}$	G_P	——	16	——	dB
Drain Efficiency@P_{SAT}	η_D	——	60	——	%
Saturated Power 4dB compression point	P_{SAT}	——	59	——	dBm
Input Return Loss	IRL	——	-4	——	dB

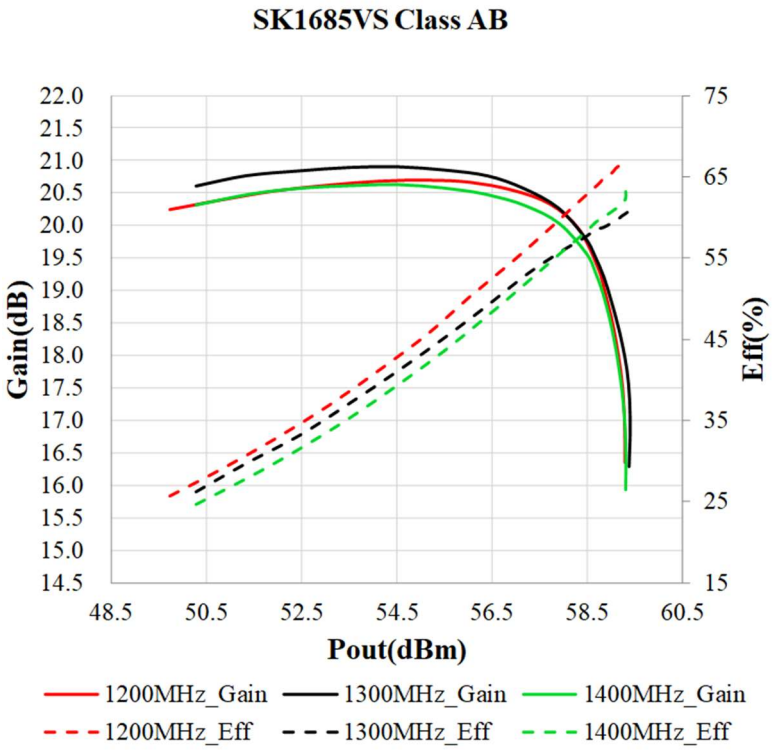
Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 50 Vdc, I_{DQ} = 100 mA, f = 1400 MHz

VSWR 10:1 at 800W pulse CW Output Power	No Device Degradation

TYPICAL CHARACTERISTICS

1.2-1.4GHz

Figure 1. Power Gain and Drain Efficiency as Function of Pulse Output Power



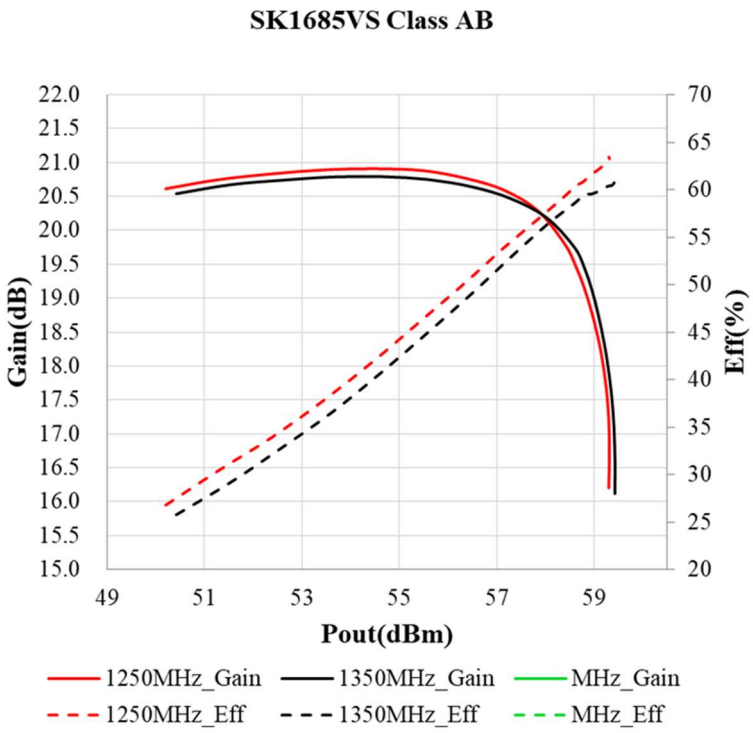


Figure 2. Network analyzer output S11/S21

VDS=50V IDQ=500mA VGS=-3.1V

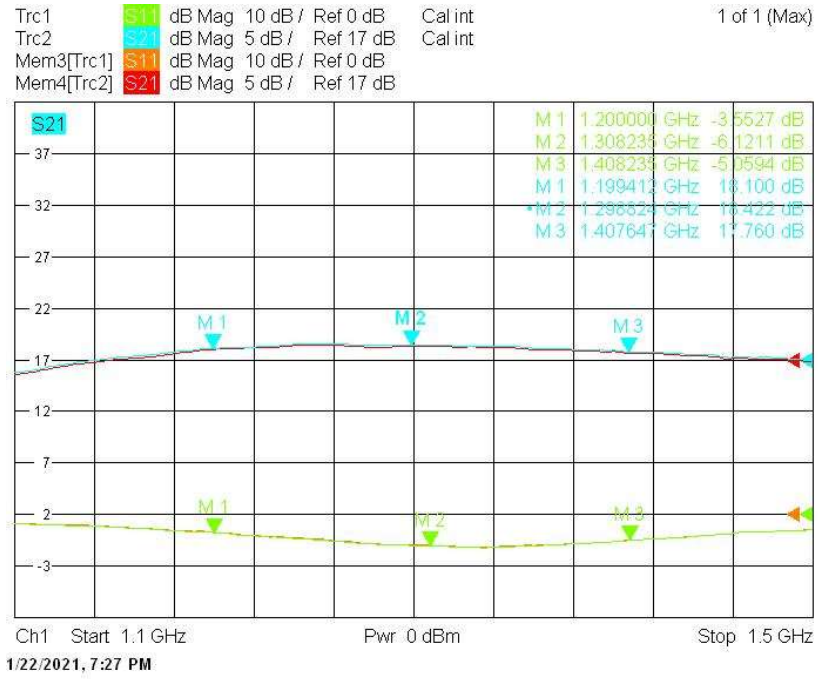


Figure 3. Test Circuit Component Layout

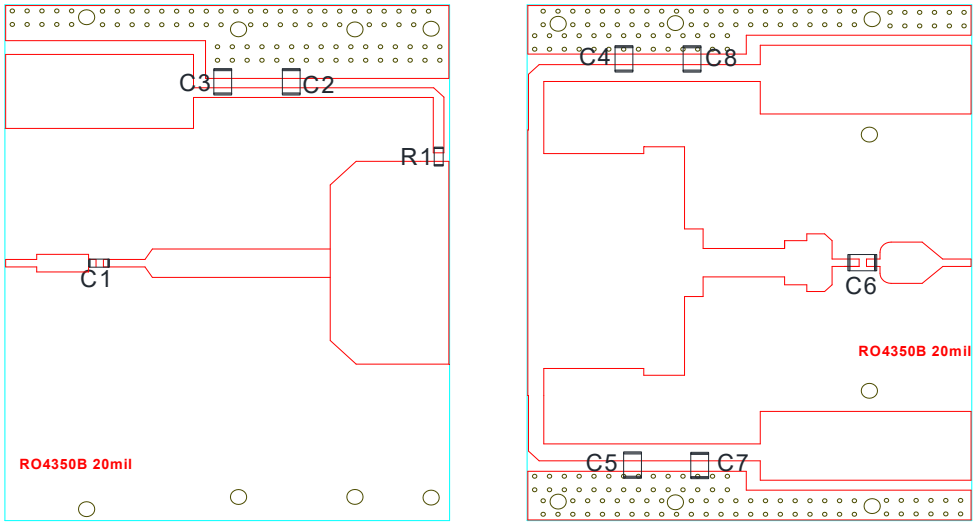


Table 4. Test Circuit Component Designations and Values

Component	Description	Suggested Manufacturer
C1	39pF	DLC75D
C2,C4,C5	56pF	DLC70B
C6	47pF	ATC800B
C3,C7,C8	10uF	10uF/50V
R1	Chip Resistor,9.1ohm	1206

1.2-1.6GHz

Figure 4. Network analyzer output S11/S21

VDS=50V IDQ=500mA VGS=-3.1V

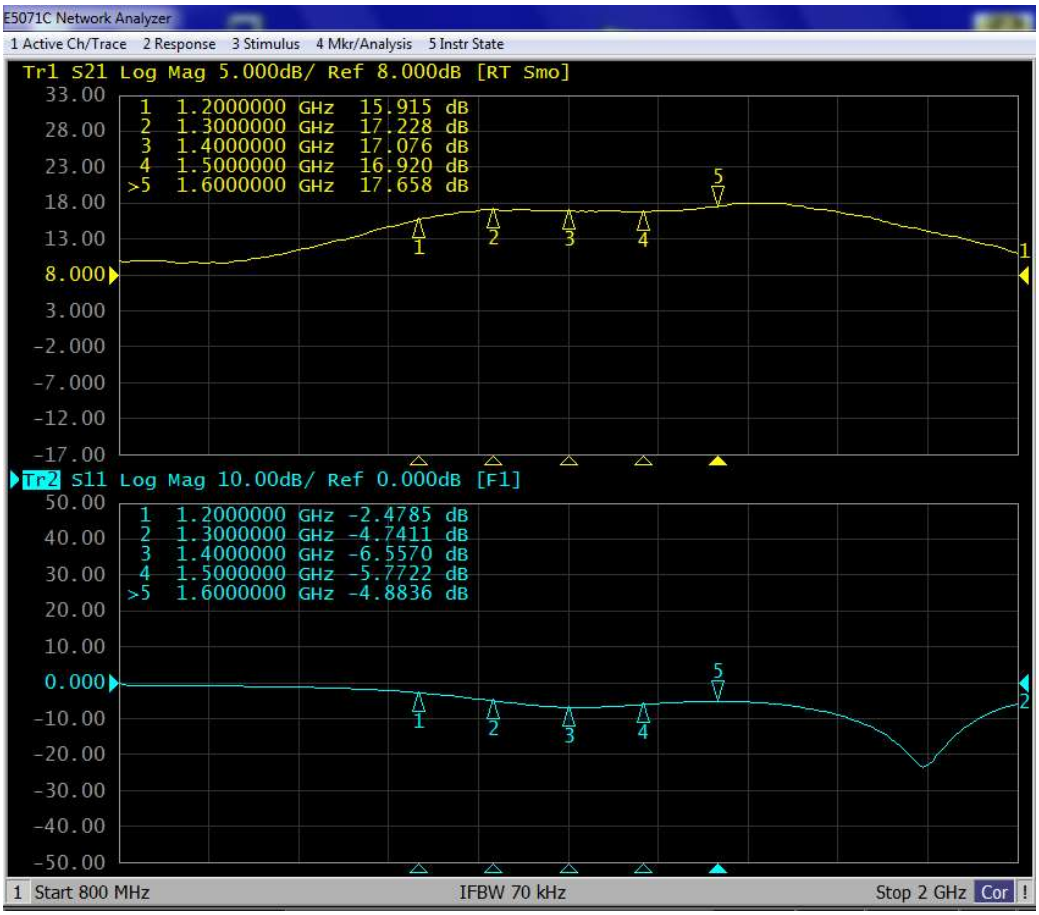


Figure 5. Test Circuit Component Layout

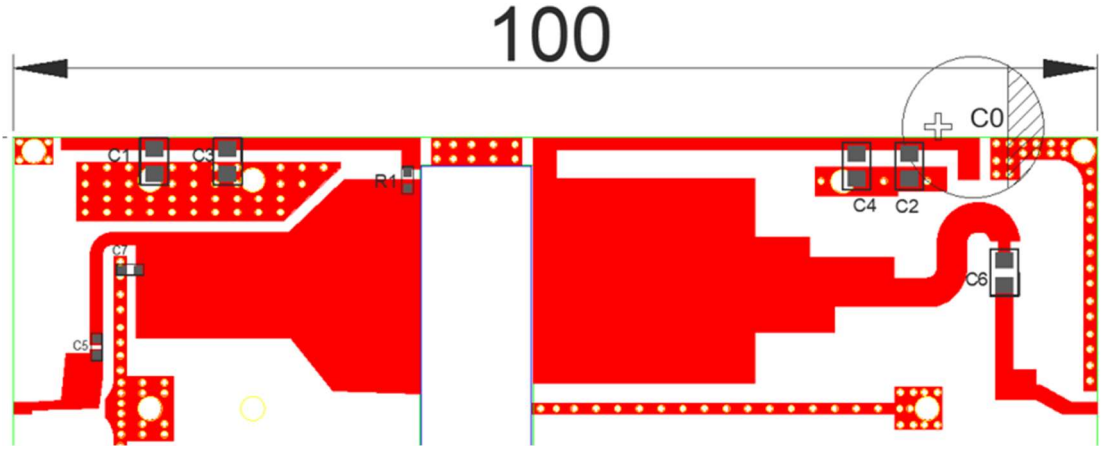


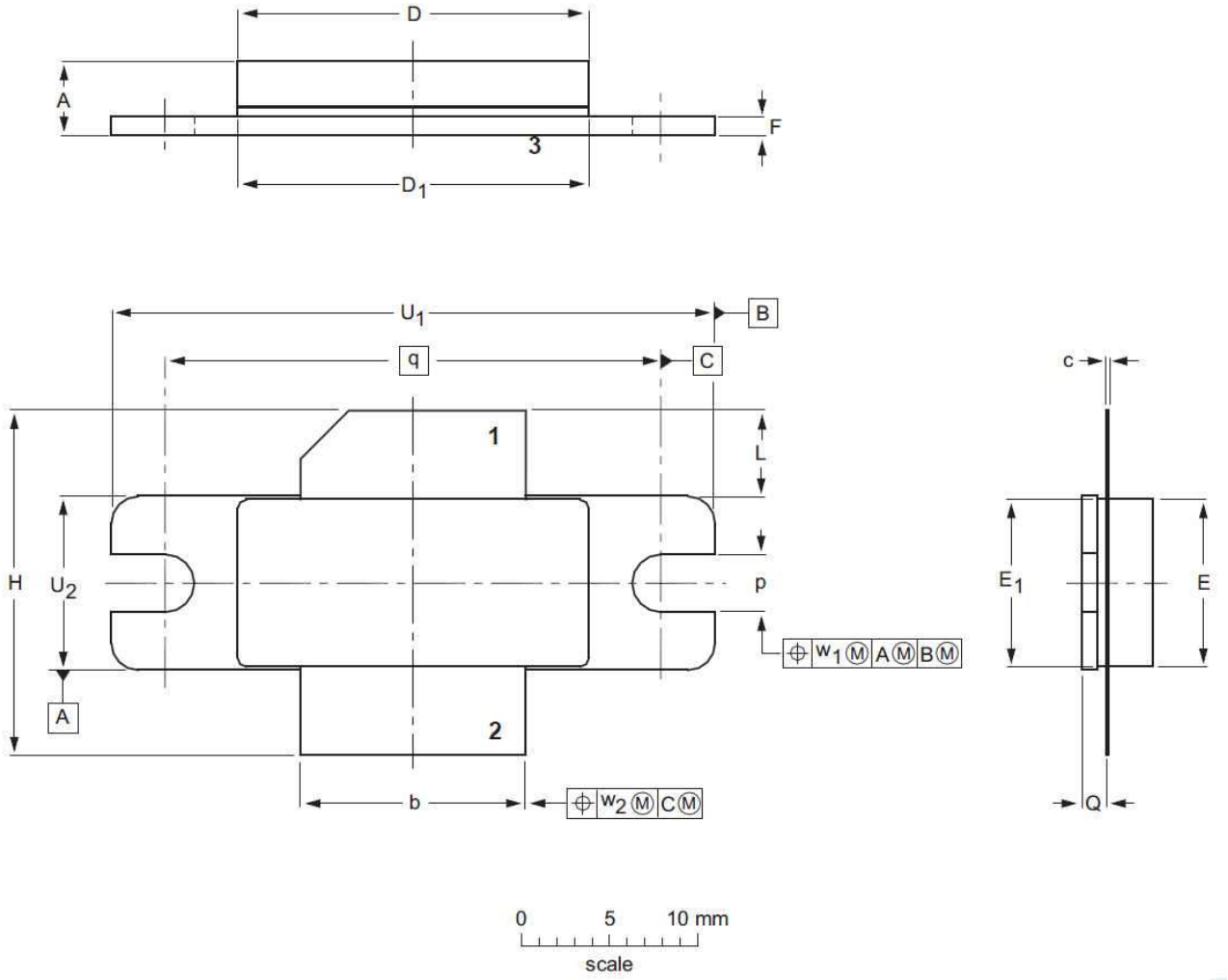
Table 5. Test Circuit Component Designations and Values

Component	Description	Suggestion
C0	4700uF/63V	
C1,C2	10uF	1210

C3,C4,C6	30pF	MQ101111
C5	30pF	DLC75D
C7	1.2pF	DLC75D
R1	Chip Resistor,9.1Ω	1206
PCB	20 Mil Rogers 4350B	

Package Outline

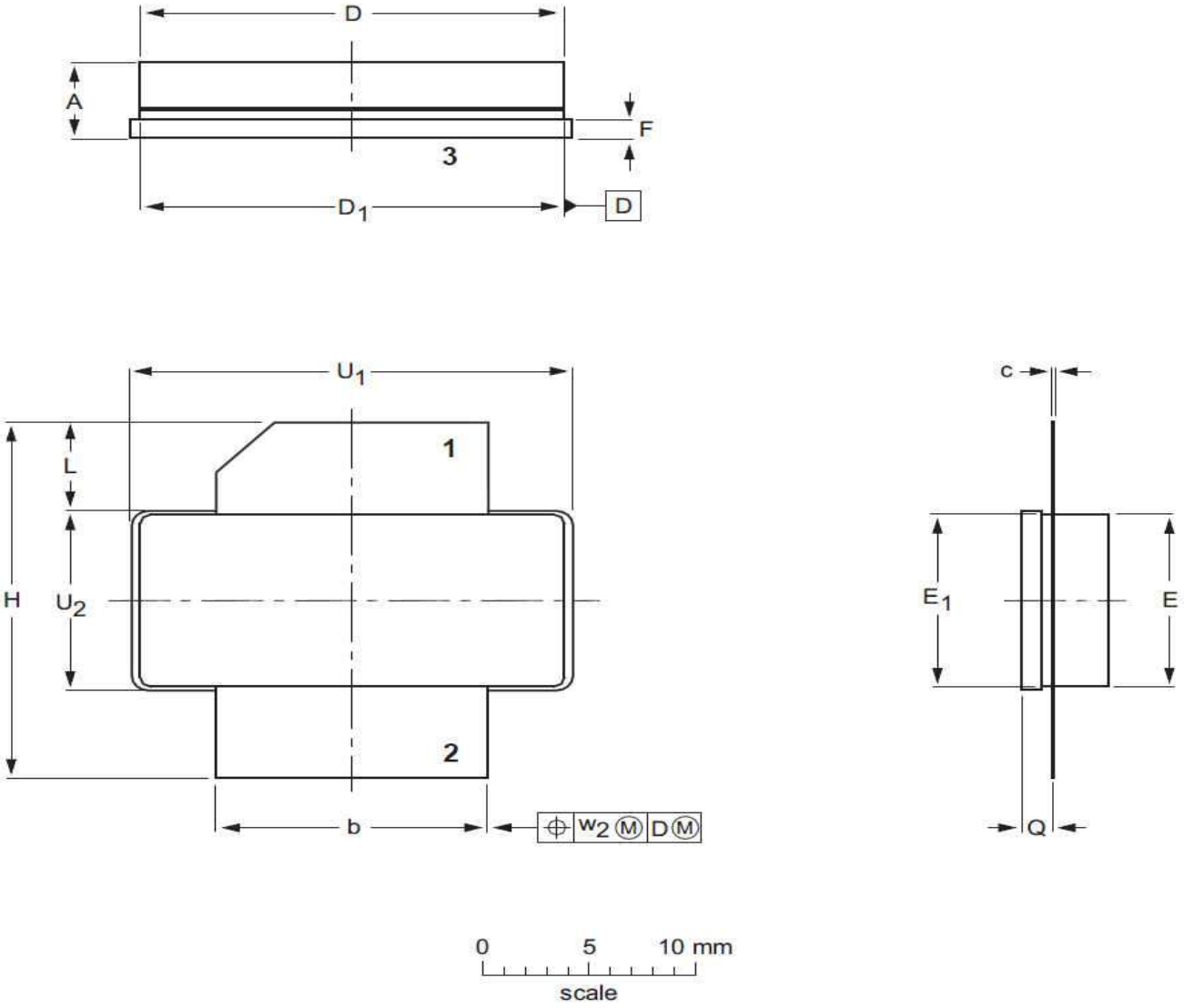
Flanged ceramic package; 2 mounting holes; 2 leads（1—DRAIN、2—GATE、3—SOURCE）



UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	W_1	W_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B2E					03/12/2013

Earless flanged ceramic package; 2 leads（1—DRAIN、2—GATE、3—SOURCE）



UNIT	A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	W_2
mm	4.72	12.83	0.15	20.02	19.96	9.50	9.53	1.14	19.94	5.33	1.70	20.70	9.91	0.25
	3.43	12.57	0.08	19.61	19.66	9.30	9.25	0.89	18.92	4.32	1.45	20.45	9.65	
inches	0.186	0.505	0.006	0.788	0.786	0.374	0.375	0.045	0.785	0.210	0.067	0.815	0.390	0.010
	0.135	0.495	0.003	0.772	0.774	0.366	0.364	0.035	0.745	0.170	0.057	0.805	0.380	

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B2					03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2021/1/26	Rev 1.0	Preliminary Datasheet,
2023/5/8	Rev 1.1	Add 1.2-1.6GHz application data

Application data based on ZL-21-05/RXT-23-14

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