

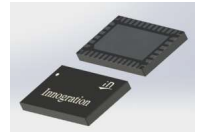


0.1-4.5GHz, 1W, 28V LDMOS 2-stage Fully matched PA Module

Description

The I2MEH0145-1 is a 1-watt,2-stage integrated Power Amplifier Module, designed for broadband applications, with frequencies from 0.1 to 4.5GHz by simple external connection between 2 stages. The module is 50 Ω input/output matched and requires minimal external components.

The module implements distributed power amplifier in form of multi chips, housed in cost effective plastic open cavity package, offers a much lower cost than traditional MMIC solutions.



- Typical CW RF performance with device soldered on PCB with high density grounding vias

$V_{DS}= 28V, I_{DQ}=40 mA, V_{GS} =2.80V$

Parameter	100MHz	0.5GHz	1.0GHz	1.5GHz	2.0GHz	2.5GHz	3.0GHz	4.0GHz	4.5GHz	Units
Linear Gain	19.4	17.4	17.0	16.4	17.9	18.0	18.4	18.3	16.7	dB
Pout@Pin=15dBm	1.7	1.5	1.4	1.1	1.3	1.3	1.3	1.4	1.2	W
Gain@Pin=15dBm	17.1	16.8	16.3	15.6	16.2	16.1	16.0	16.6	16.0	dB
Eff@ Pin=15dBm	21	19	17	15	18	18	17	21	21	%

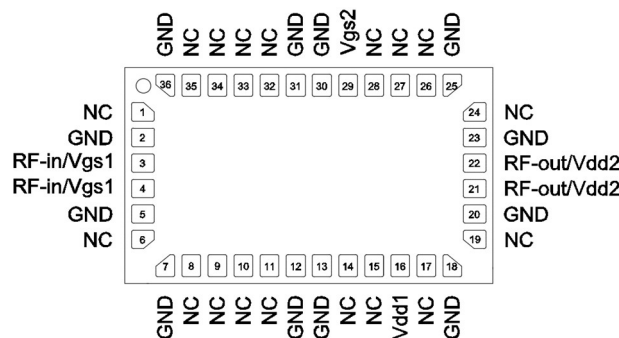
Product Features

- Operating Frequency Range: 0.1-4.5GHz
- Operating Drain Voltage: +28 V
- 50 Ω Input/Output
- Psat: ≥1W(CW)
- Small signal gain:>16dB
- Minimum efficiency:>15%
- 6x10 mm Surface Mount Package
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC
- Much lower cost than GaN-based ultrawide band PA , due to LDMOS technology used

Applications

- Ultra Broadband Amplifiers
- Fiber Drivers
- Test Instrumentation
- EMC Amplifier Drivers
- 2-way Radios

Pin Configuration and Description



Pin No.	Symbol	Description
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21,22	RFout/Vdd2	Transistor 1, Drain Bias2 & RF Output
3,4	RFin/Vgs1	Transistor 1, Gate Bias1 & RF Input
29	Vgs2	Transistor 1, Gate Bias2
16	Vdd1	Transistor 1, Drain Bias1
Others	NC	No connection
2,5,7,12, 13,18,20,23,25, 30, 31,36 Package Base	GND	DC/RF Ground. Must be soldered to EVB ground plane over array of vias for thermal and RF performance. Solder voids under Pkg Base will result in excessive junction temperatures causing permanent damage.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_j	+200	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_c=87^\circ\text{C}$, $T_j=175^\circ\text{C}$, DC test	$R_{\theta JC}$	14	°C/W

Table 3. Electrical Characteristics

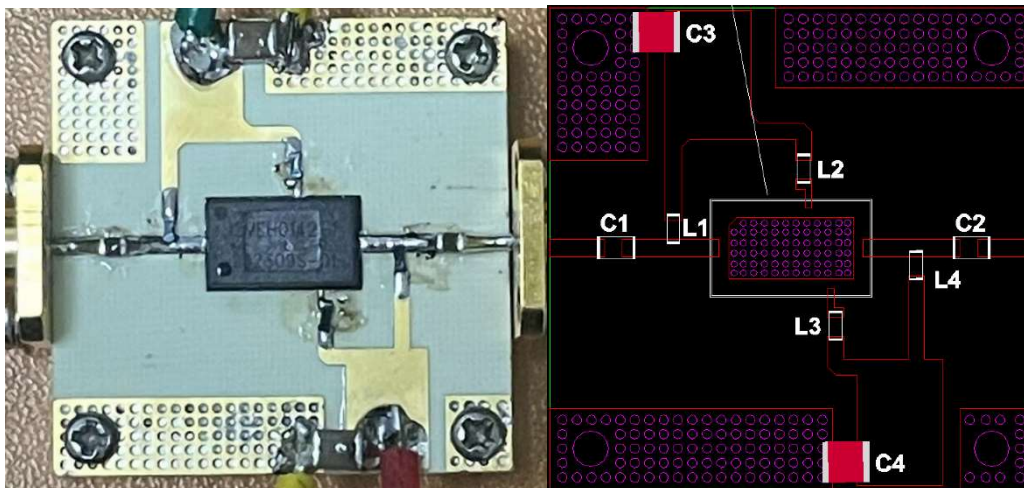
Parameter	Condition	Min	Typ	Max	Unit
Frequency Range		30		4000	MHz
Power Gain @ Psat			21		dB
P_{SAT}		30			dBm
Drain Efficiency @ P_{SAT}		15			%

Unless otherwise noted: $T_A = 25^\circ\text{C}$, $V_{DD} = 28\text{ V}$, Pulse Width=100 us, Duty cycle=10%

Load Mismatch of per Section (On Test Fixture, 50 ohm system): $V_{DD} = 28\text{ V}$, $I_{DQ} = 100\text{ mA}$, $f = 3\text{ GHz}$

VSWR 10:1 at Psat pulse CW Output Power	No Device Degradation
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Reference Circuit of Test Fixture Assembly Diagram





		Part NO.	Vendor
C1, C2	50V 1uF Chip Capacitor	GRM21BR71H105KA12L	muRata
C3,C4	10uF 100V Chip Capacitor	C5750X7S2A106M230KB	TDK
L1, L2,L3,L4	470 nH Capacitor(0603)	LQW18CNR47J00D	muRata
PCB	RO4350B,20mil,er=3.48		

TYPICAL CHARACTERISTICS

Figure 1. Network analyzer output S11/S21 (Pin=0dBm)

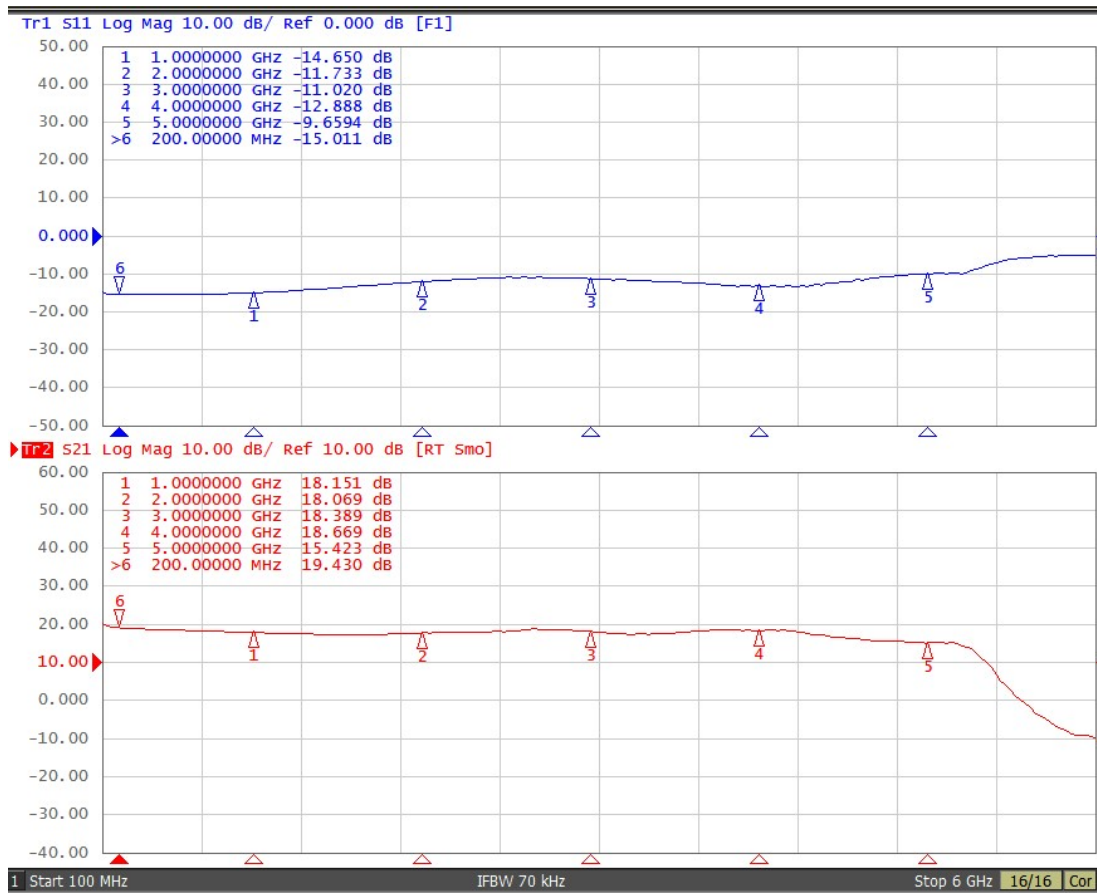
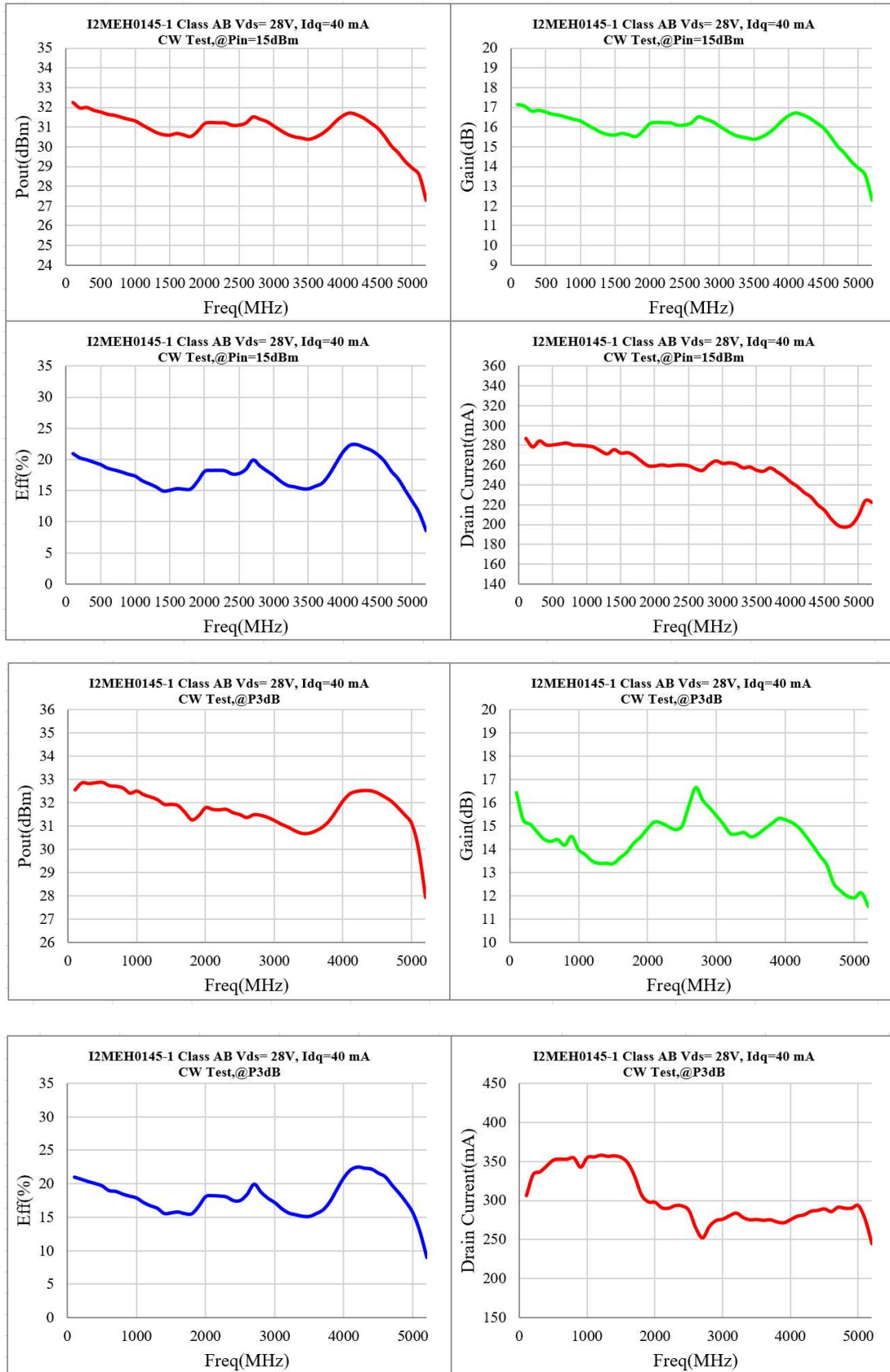


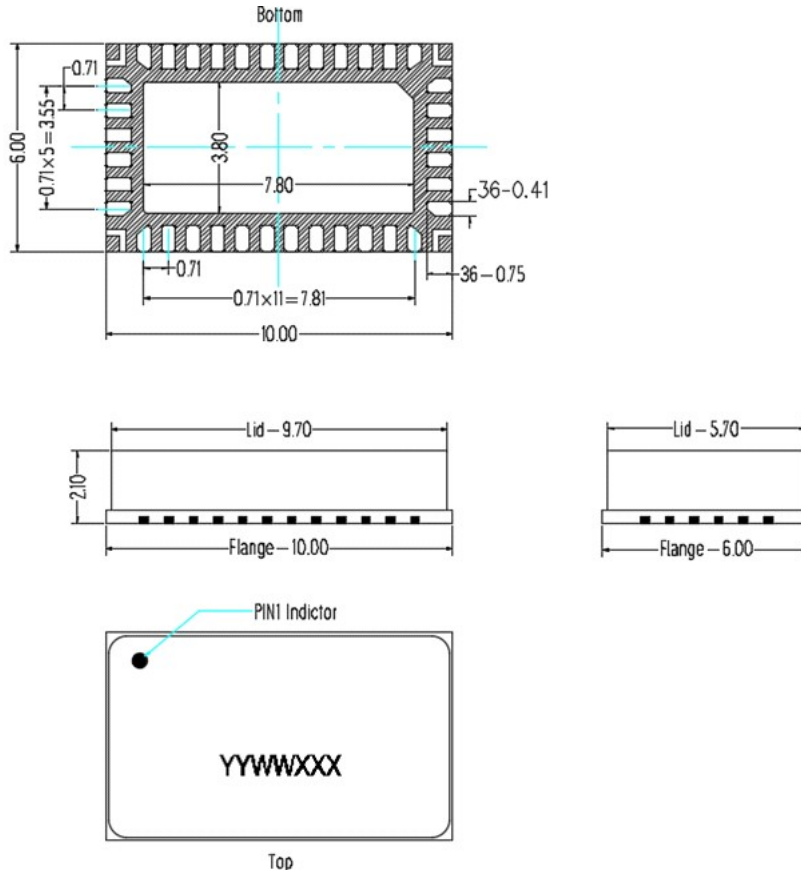


Figure. Power Gain and, efficiency and Pout @different Idq/Pin=15dBm ,and P3dB vs. Frequency



Package Dimensions

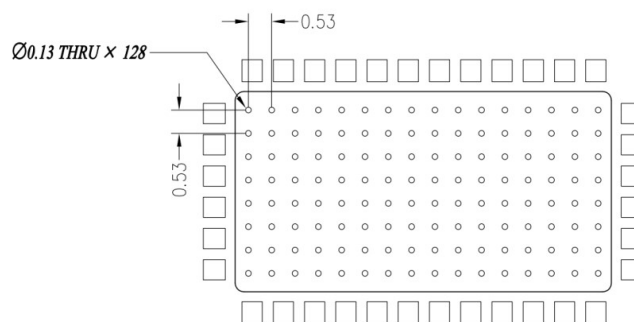
10*6 Plastic Package



Notes:

1. All dimensions are in mm;
2. The tolerances unless specified are ± 0.2 mm.

Mounting Footprint Pattern



Notes:

1. All dimensions are in mm;
2. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. ALL vias are PTH to ground.



Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2023/6/8	Rev 1.0	Production Datasheet

Application data based on ZHH-23-09

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