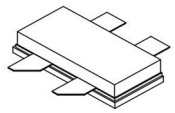
GaN HEMT 50V, 600W,2.3-2.4GHz RF Power Transistor

Description

STCV24600BY4



The STCV24600BY4 is a dual path 600watt , Input matched GaN HEMT, ideal for applications from 2.3 to 2.4GHz especially for LTE/5G

There is no guarantee of performance when this part is used outside of stated frequencies.

- Typical RF performance on asymmetrical Doherty with device soldered

VDS= 50V, IDQ=100mA(Vgm=-3.3V，Vgp=-5.70V)

Pulsed CW: 20uS width, 10% cycle.

Freq (MHz)	Pulse CW Signal				P_{avg}=49dBm WCDMA Signal		
	P1 (W)	P1 gain (dB)	P3 (W)	P3 Eff (%)	Gp (dB)	Eff (%)	ACPR5M (dBc)
2300	596.9	14.55	720.8	71.5	14.8	52.5	-32.3
2350	575.8	14.3	692.4	74.4	14.4	53.0	-29.2
2400	466.3	13.89	612.7	75.7	14.1	53.4	-29.7

Applications

- Asymmetrical Doherty amplifier within 2.3-2.4GHz
- S band power amplifier
- CW or pulsed Amplifier

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically –5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically –5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Figure 1: Pin Connection definition

Transparent top view (Backside grounding for source)

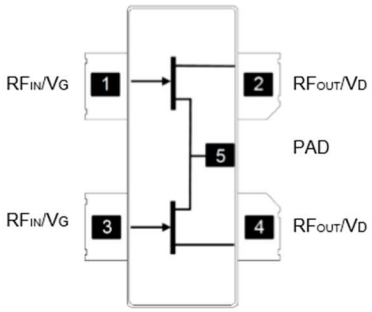


Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum gate current	Igs	77	mA

Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA T_C= 85°C, at Pd=90W, on Doherty application board	$R_{\theta JC}$	0.85	°C /W

Table 3. Electrical Characteristics (TA = 25℃ unless otherwise noted)

DC Characteristics (Main path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=30mA	V_{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 30mA	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	VDS =50V, IDS=100mA, Measured in Functional Test	$V_{GS(Q)}$		-3.3		V

DC Characteristics (Peak path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=47mA	V_{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 47mA	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	VDS =50V, IDS=150mA, Measured in Functional Test	$V_{GS(Q)}$		-3.3		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	2.35GHz, Pout=80W WCDMA 1 Carrier in Doherty circuit All phase, No device damages	VSWR		10:1		

Figure 2: Median Lifetime vs. Channel Temperature

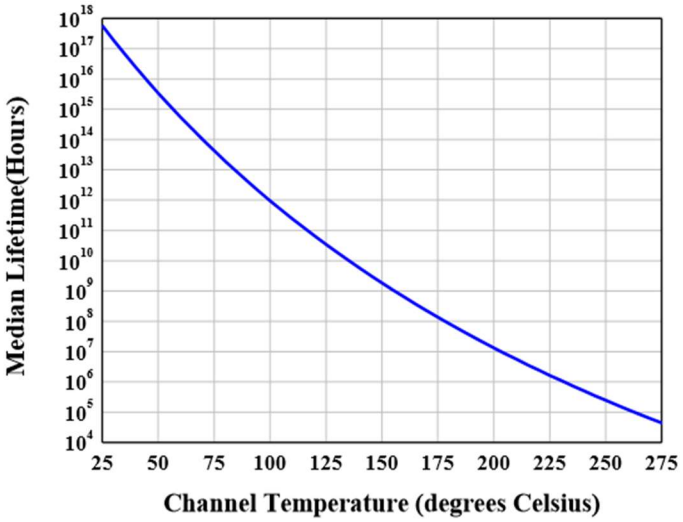


Figure 3: Efficiency and power gain as function of Pout

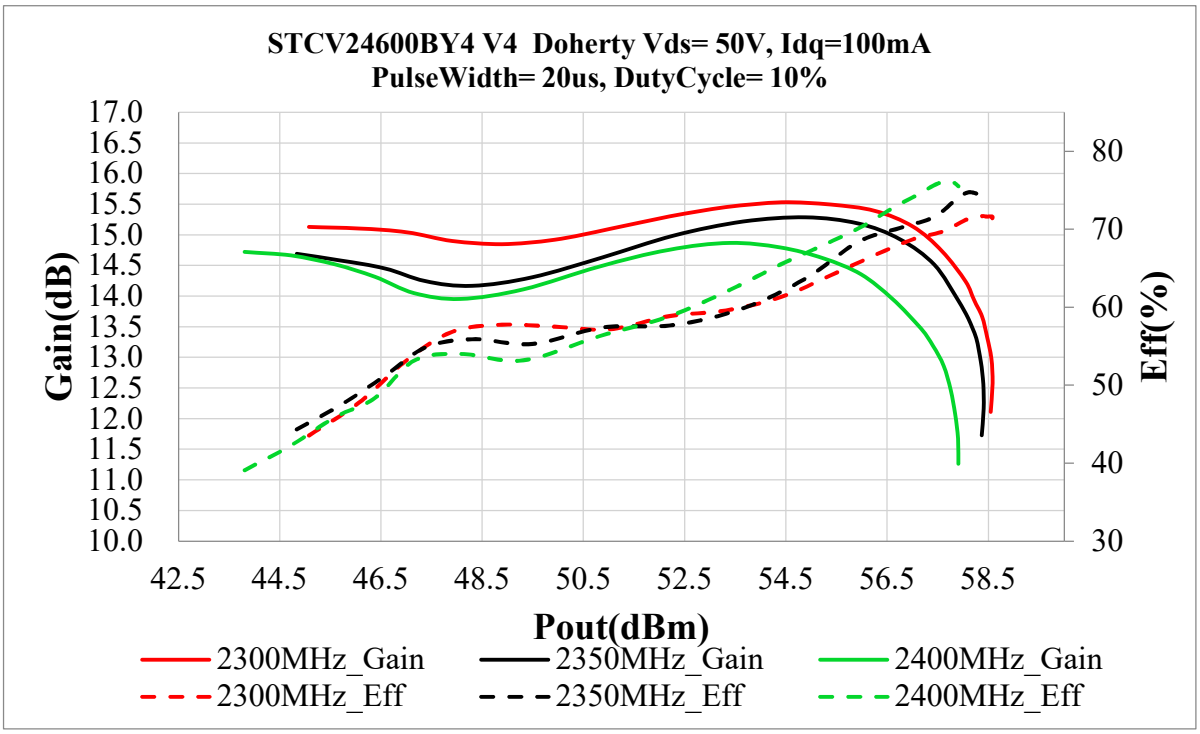


Figure 4: Network analyzer output, S11 and S21

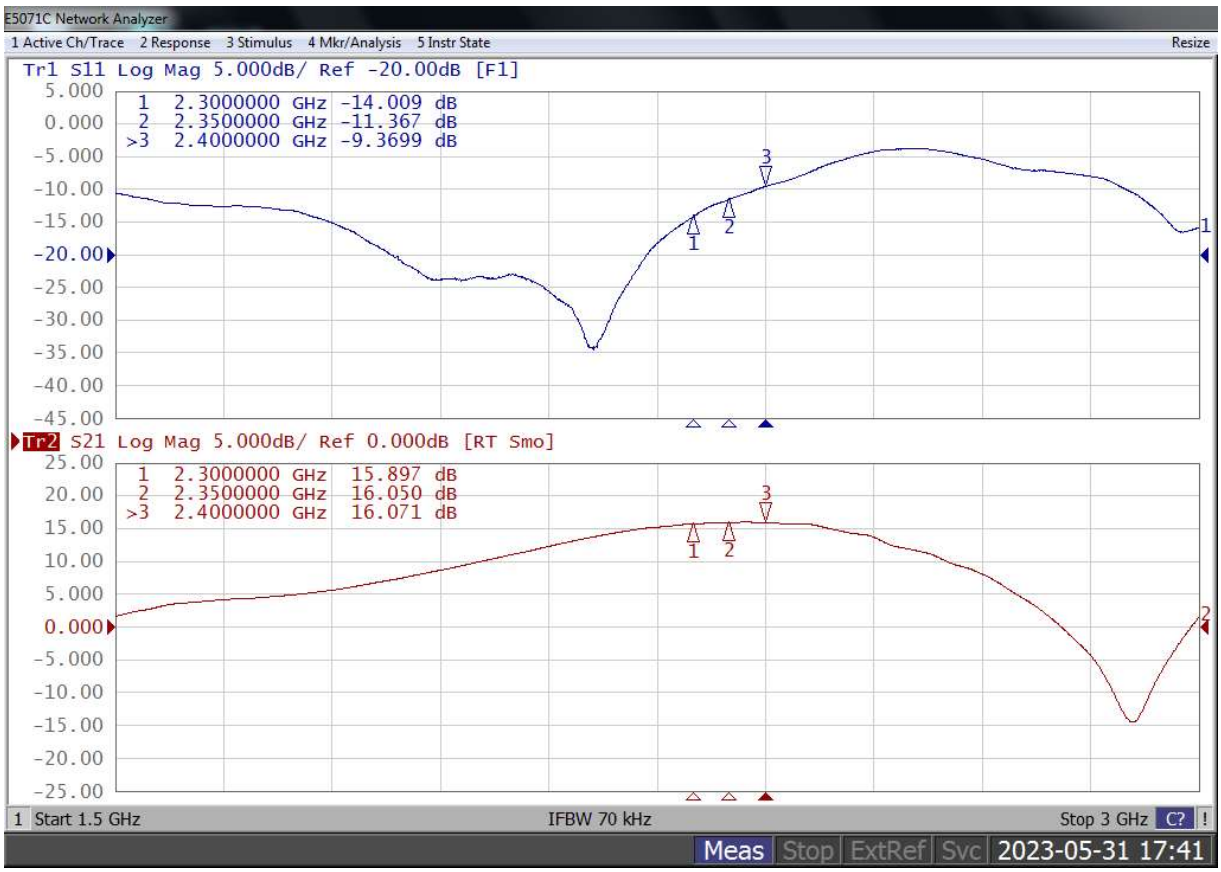


Figure 5: Picture of application board Doherty circuit

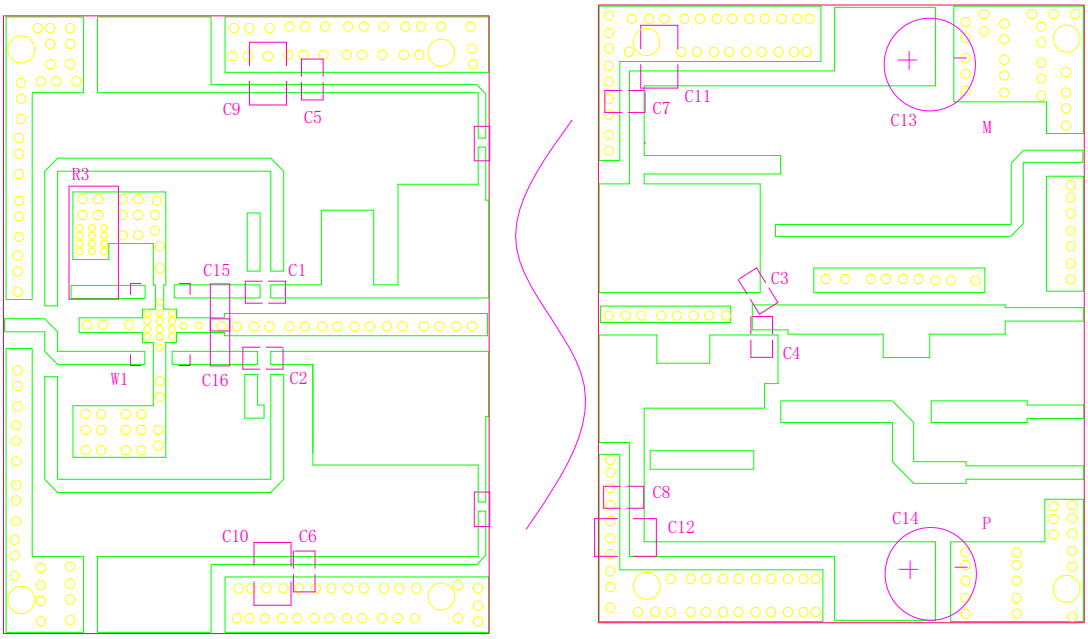
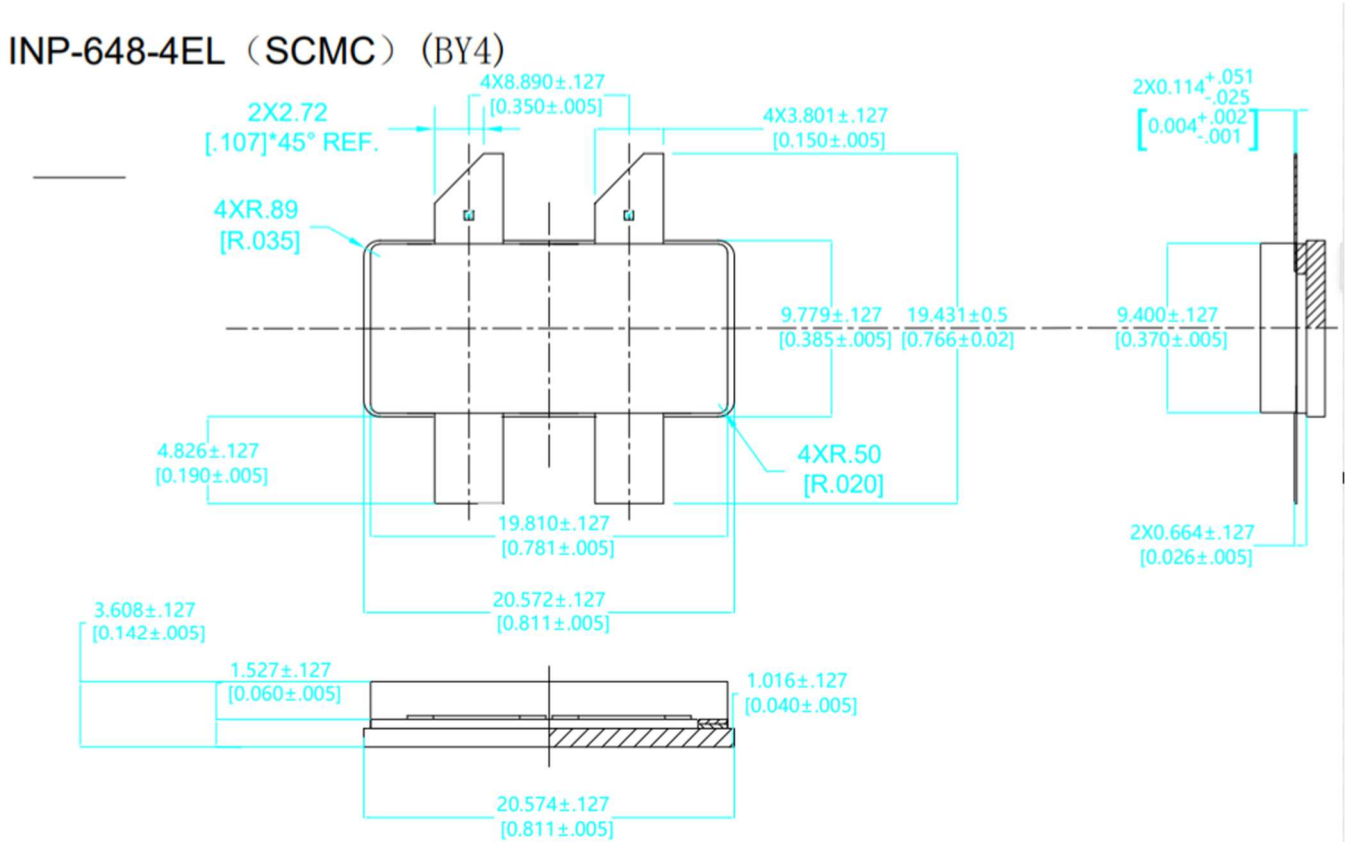


Table 4. Bill of materials of application board (PCB layout upon request, RO4350B 20mils)

Designator	Comment	Footprint	Quantity
C1, C2, C5, C6, C7, C8	15 pF	0603/0805	6
C3	2 pF	0603	1
C4	10pF	0805	1
C9, C10, C11, C12	10 uF/100V	1210	4
C13, C14	100 uF/63V		2
C15	0.2pF	0603	2
C16	0.5pF	0603	1
R1, R2	10 Ω	0603	1
R3	51 Ω	2512	1
W1	HC2100P03		1

Earless Flanged Ceramic Package; 4 leads



Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2023/6/1	**V1.0**	**Preliminary Datasheet Creation**
2023/12/28	**V1.1**	**Modify the drawing for lead width for BY4**

Application data based on: LSM-23-18

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