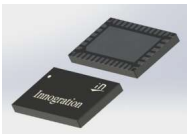
20W,13.6V High Power RF LDMOS FETs

ITEH09070C6



Description

The ITEH09070C6 is a 20-watt, highly rugged, unmatched LDMOS FET, designed for commercial and industrial applications at frequencies up to 1GHz. It can be used in linear or saturated power amplifier, for CW and pulsed signal, and any modulation format.

It is also featured by its lower cost of plastic open cavity for surface mount on PCB through vias

- Typical LMR UHF CW Performance (On Innogration fixture with device soldered).

ITEH09070C6 Vds=13.6V Idq=170mA Vgs=2.6V CW						
F(MHz)	Pin（dBm）	Psat（dBm）	Psat（W）	I(A)	Gain（dB）	Eff(%)
400	25.3	43.20	21	2.55	17.9	60.2
410	25.4	44.00	25	2.77	18.6	66.7
420	24.8	43.70	23	2.53	18.9	68.1
430	24.7	43.10	20	2.24	18.4	67.0
440	24.7	43.00	20	2.10	18.3	69.9
450	25	43.00	20	2.10	18.0	69.9
460	25.5	42.64	18	1.95	17.1	69.3
470	26	42.20	18	1.78	16.2	68.6

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- VHF/UHF Land mobile radio (LMR)
- RF Energy application at ISM bands

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+70	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+28	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	RθJC	0.8	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0, I_{DS}=100uA	$V_{(BR)DSS}$		70		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 13.6V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 9 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 13.6V, I_D = 600 μA)	$V_{GS(th)}$	——	2	——	V
Gate Quiescent Voltage (V_{DD} = 13.6V, I_D = 170mA, Measured in Functional Test)	$V_{GS(Q)}$	——	2.6	——	V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 13.6Vdc, I_{DQ} = 170 mA, f = 1000 MHz

VSWR 10:1 at 20W pulse CW Output Power	No Device Degradation

Figure 1:Pin Definition(Top View)

Pin No.	Symbol	Description
1-7,12,13,18-25,30,31,36	GND	DC/RF Ground
8,9,10,11,14,15,16,17	Vgs/RF In	Vgs and RF input
26,27,28,29,32,33,34,35	Vds/RF out	Vds and RF output
Package Base	GND	DC/RF Ground.

Reference Circuit of Test Fixture Assembly Diagram
400-470MHz RO4350B 30mils

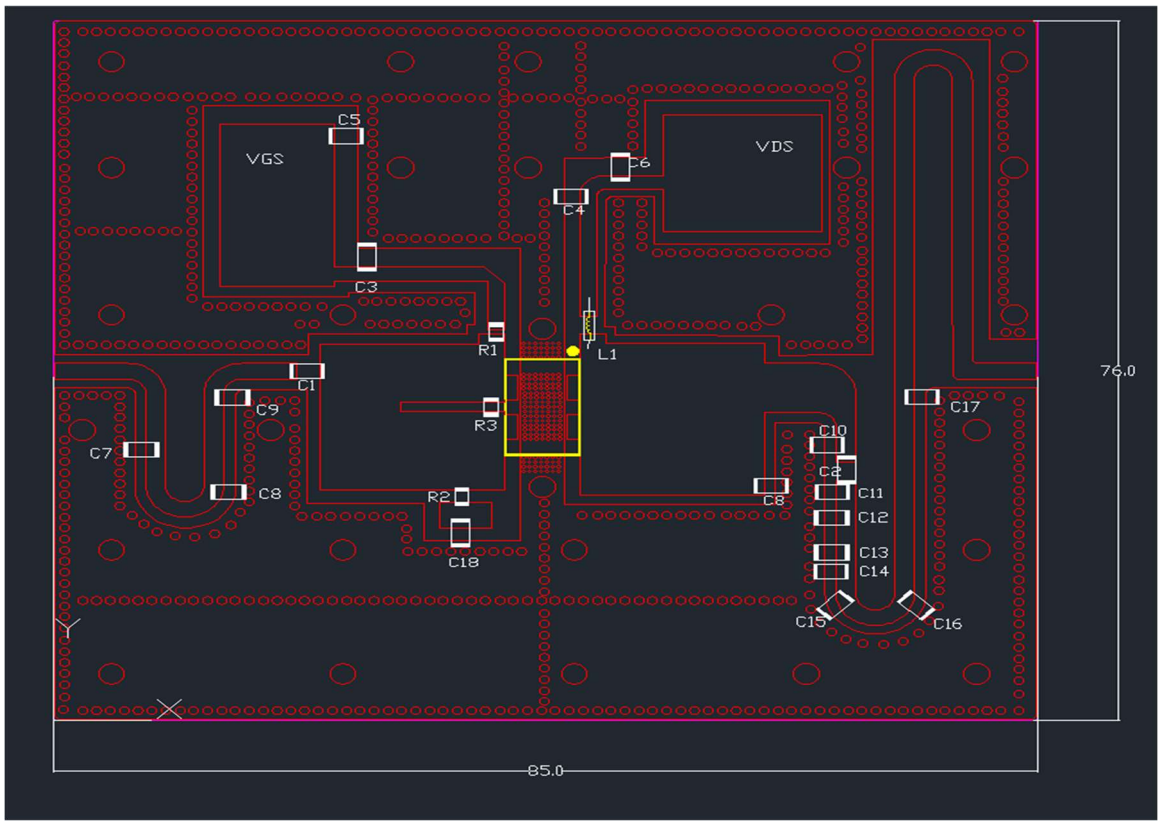


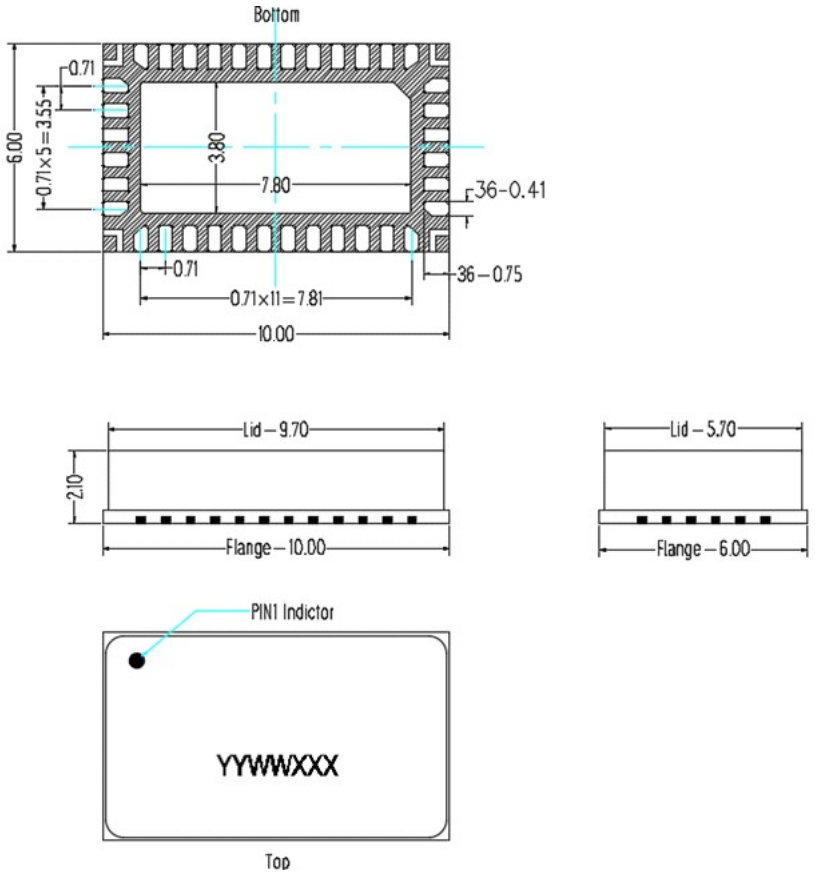
Figure 5. Test Circuit Component Layout

Table 5. Test Circuit Component Designations and Values

Component	Description	Suggestion
C1,C2,C4	120pF	MQ101111
C3	120pF	MQ101111
C5,C6,C18	10uF 100V	Ceramic multilayer capacitor
C7	10pF	MQ101111
C8,C15,C16	5.1pF	MQ101111
C9	20pF	MQ101111
C10,C17	3.9pF	MQ101111
C11	4.3pF	MQ101111
C12	2.7pF	MQ101111
C13	1.5pF	MQ101111
C14	3.0pF	MQ101111
R1	9.1 ohm 1206	Ceramic multilayer capacitor
R2	5.1 ohm 1206	Ceramic multilayer capacitor
R3	51*3 ohm 1206	Ceramic multilayer capacitor
PCB	30Mil Rogers4350	

Package Dimensions

10*6 Plastic Package



Notes:

1. All dimensions are in mm;
2. The tolerances unless specified are ±0.2mm.

Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2023/6/13	**Rev 1.0**	**Preliminary Datasheet**

Application data based on SXY-23-24

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