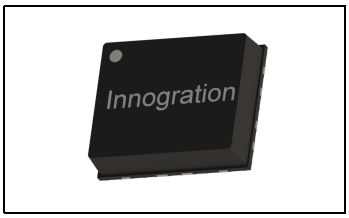
3.7-4GHz, 200W, 50V GaN matched PA Module



Description

The SMBV3740-201 is a 200-watt, integrated 2-stage Power Amplifier Module, designed for 5G massive MIMO applications, with frequencies from 3.7 to 4GHz. The module is 50 Ω input fully matched and output partially matched, and requires minimal external components. The module offers a much smaller footprint than traditional discrete component solutions，with much less sensitivity for production, housed in 12*10mm cost effective plastic open cavity package, and heat dissipated by copper flange.

The module incorporates advanced Doherty circuit delivering high power added efficiency for the entire module at 28W average power according to normal 8.5 dB back off.

Innogration owns the patents for internal Doherty architecture, and related plastic open cavity.

- Typical Performance of 3.7-4G Full band Doherty (On Innogration fixture with device soldered on copper coin directly):

VDS=**50**V, IDQ-main=140mA Vgs-main=-3.12V. Vgs-peak=-5.2V, Idq-driver=48mA, Vgs-Driver=-3.14V

Freq (GHz)	Pulse CW Signal(1)			Pavg=44.5dBm WCDMA Signal(2)		
	P1-Gain (dB)	P5 (dBm)	P5 (W)	Gp (dB)	Eff (%)	ACPR5M (dBc)
3.7	29.95	53.47	222	29.64	42.86	-28.04
3.8	30.51	53.45	221	29.90	42.31	-29.45
3.9	30.55	53.40	218	29.61	42.40	-28.58
4.0	30.23	52.96	197	29.53	42.45	-27.82

Notes:

(1) Pulse Width=20 us, Duty cycle=10%
(2) WCDMA signal: 3GPP test model 1; 1 to 64 DPCH; Channel Bandwidth=3.84MHz,PAR =10.5 dB at 0.01 % probability on CCDF.

Features and Benefits

- Adjustable drain bias to fit different power demand
- Extremely good VBW performance to enable the broadest IBW/OBW
- Industry leading RF performance for 5G MIMO AAU, for instance

✓ 32T:640W / 300MHz

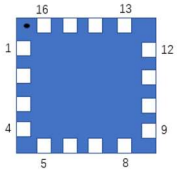
- Plastic open cavity without molding compound brings advantage compared to molded design

✓ Minimize the risk of high density thermal distribution in fanless system for longer life time

✓ Highly consistent RF performance for yield of volume production

- 50 Ω Input matched, output partially matched, total effective PCB space smaller than 25*35mm
- Integrated Doherty Final and driver Stage
- 12*10 mm Surface Mount Package, full copper flange underneath for grounding and heat dissipation, much more effective than LGA PCB based design

Pin Configuration and Description （Top view）



Pin No.	Symbol	Description
3	RF IN	RF Input
1	Vds-driver	Driver stage, Drain Bias
2	Vgs-driver	Driver stage, Gate Bias
9,10	RF Out2/Vds-Main	RF Output，Drain Bias of Main Amplifier
11,12	RF Out1/Vds-Peak	RF Output, Drain Bias of Peaking Amplifier
6	Vgs-main	Main Amplifier, Gate Bias
13	VBE-peak	VBW enhancement for Peak
15	Vgs-peak	Peaking Amplifier, Gate Bias
8	VBE-main	VBW enhancement for Main
4,5,7,14,16	NC	No connection
Package Base	GND	DC/RF Ground. Must be soldered to EVB ground plane over array of vias for thermal and RF performance. Solder voids under Pkg Base will result in excessive junction temperatures causing permanent damage.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.6	Vdc
Operating Voltage	V_{DD}	+60	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance@Average Power, Junction to Case Tcase=+85℃，CW Test，Pout=25W,	$R_{\theta JC}$	1.06	°C/W

Notes:
(1) The thermal resistance is acquired by our company's FEA model,which was calibrated by IR measurement,the value shall be applied to reliability.
(2) The reference Tcase temperature 85℃ is apply on the backside of package.
(3) It is recommended to use copper coin underneath to maximize the heat dissipation.
(4) The power dissipation in the table is overall dissipation which includes Carrier PA, Peaking PA and driver PA..

Table 3. ESD Protection Characteristics

Test Methodology	Class Voltage
Human Body Model(HBM) (JEDEC Standard JESD-A114)	±200V
Charged Device Model (CDM) (JEDEC Standard JESD22-C101F)	±1000V

Table 4. Electrical Characteristics

Parameter	Condition	Min	Typ	Max	Unit
Frequency Range		3.7		4	GHz
Driver Quiescent Current (IDQ-driver)			48		mA
Carrier Quiescent Current ($I_{DQ\text{-}main}$)			140		mA
Peak PA Gate Quiescent Voltage (V_{PEAK})			-5.2		V
Power Gain @ Pout=44.5dBm	Freq=3.8GHz		29		dB

Efficiency @Pout=44.5dBm	Freq=3.8GHz		42		%
Ppeak by CCDF	Freq=3.8GHz		200		W

Load Mismatch of per Section (On Test Fixture, 50 ohm system): f = 3.8GHz

VSWR 10:1 at P5dB pulse CW Output Power	No Device Degradation

TYPICAL CHARACTERISTICS

Figure 1. Power Gain and Drain Efficiency as Function of Pulsed CW Output Power @VDS=50V

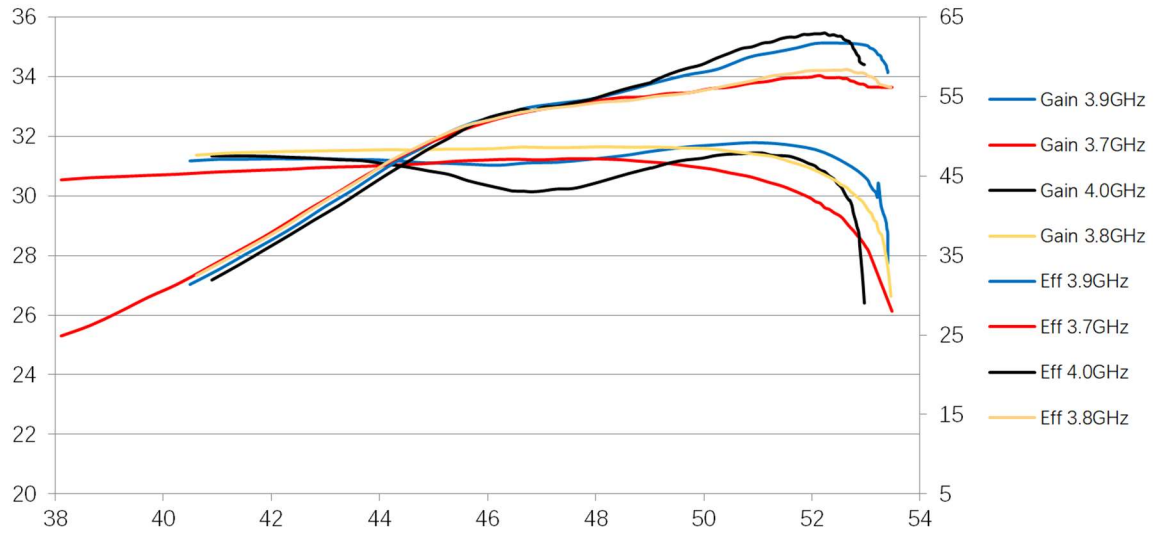


Figure 2. Network analyzer output S11/S21

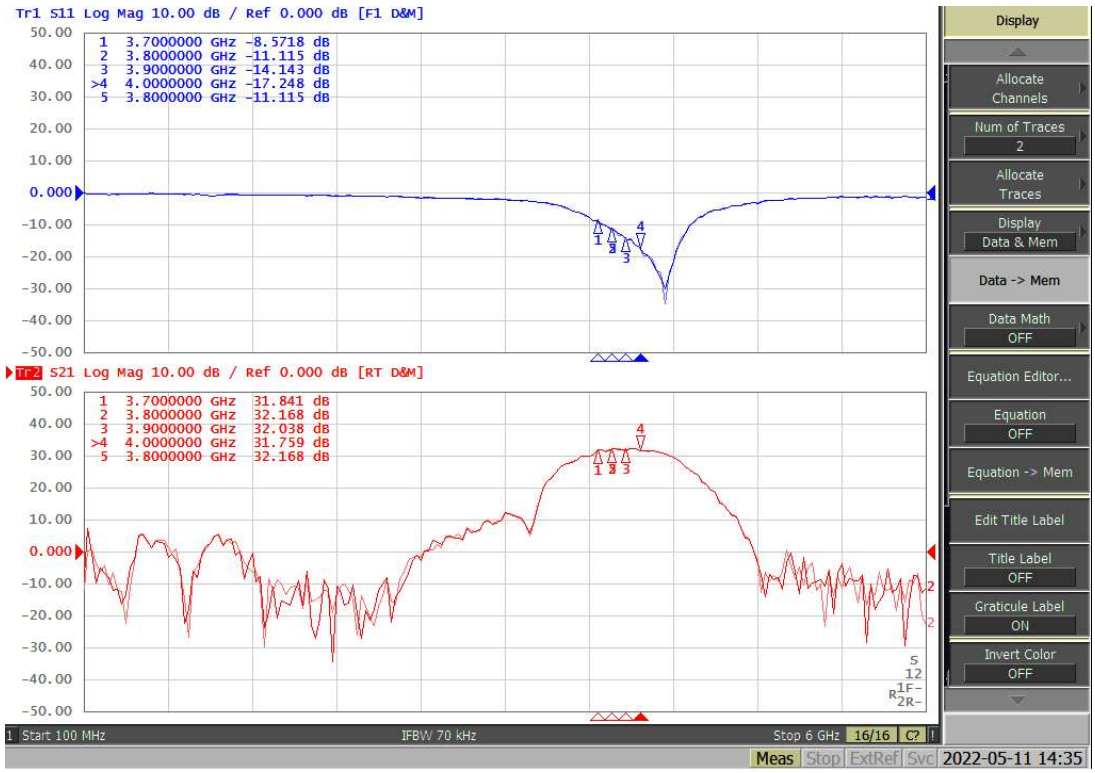


Figure 3: Intermodulation Distortion Products versus Two--Tone Spacing

Vdd=50V, Pout=44.5dBm, Center Frequency=3.8GHz

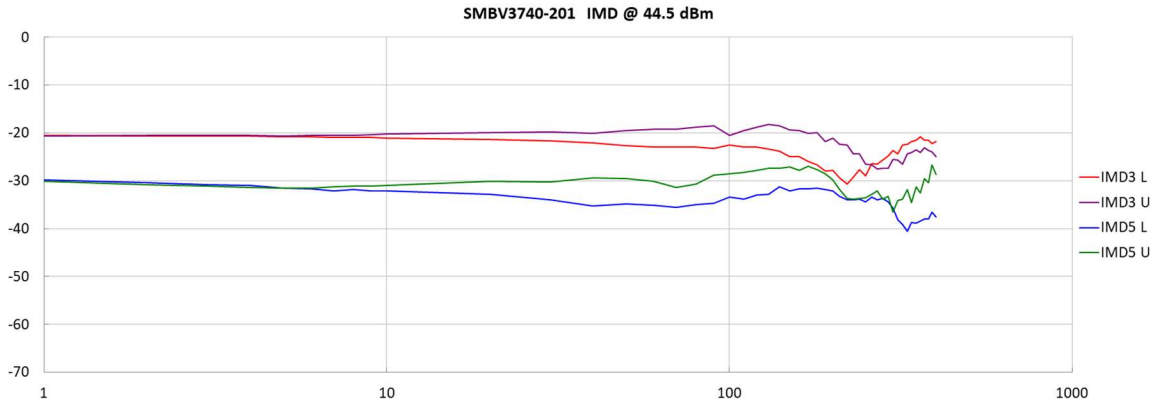


Figure 4: Picture of application board Doherty circuit for 3.7-4GHz

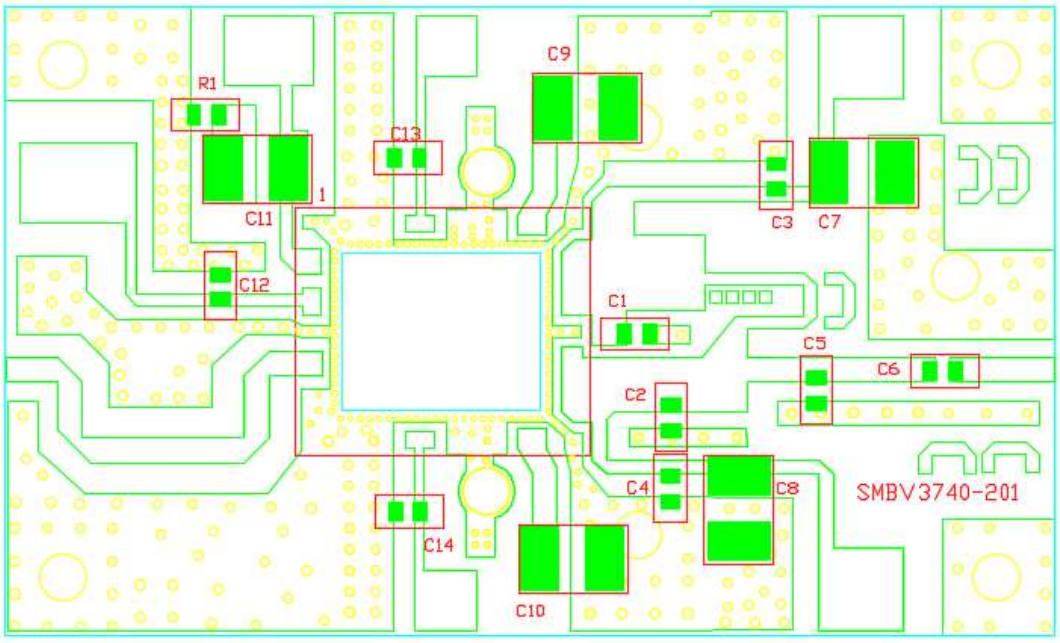
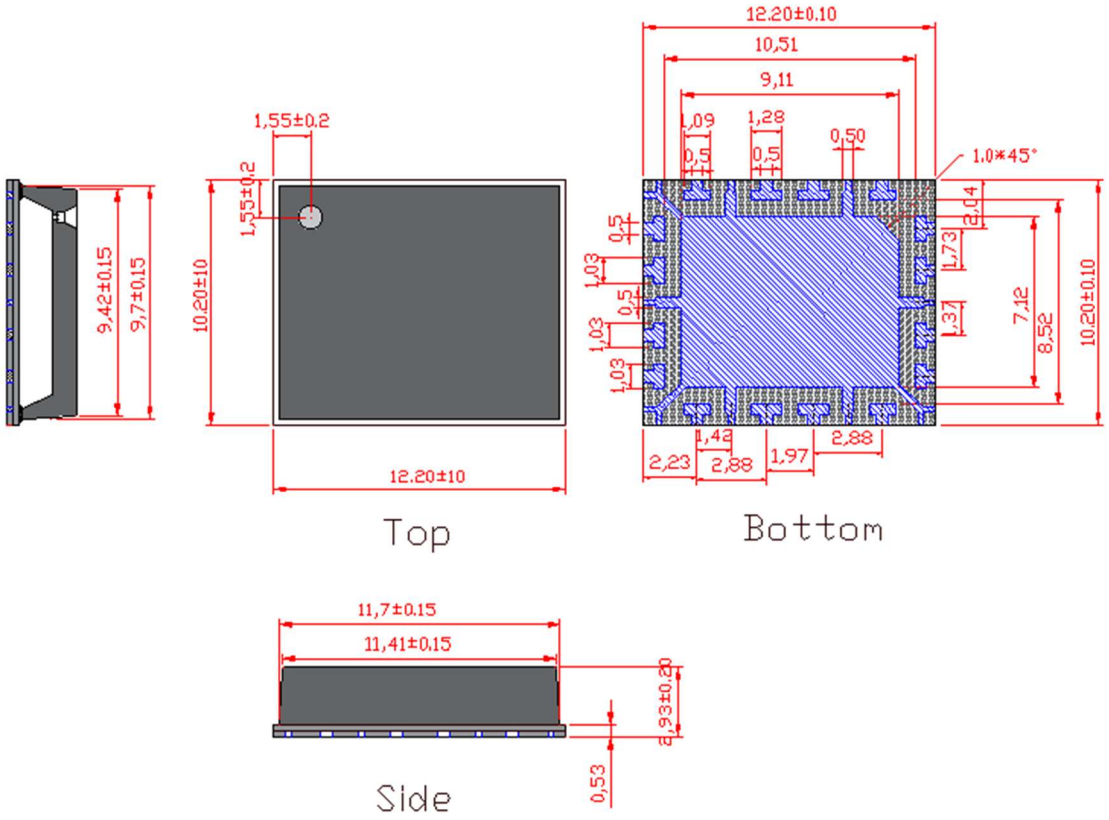


Table 4. Bill of materials of application board (PCB layout upon request, RO4350B 20mils)

Part	Quantity	Description	Part Number	Manufacture
C3,C4,C6	3	8.2pF High Q Capacitor	251SHS8R2BSE	TEMEX
C1	1	0.6pF High Q Capacitor	251SHS0R6BSE	TEMEX
C2	1	0.4pF High Q Capacitor	251SHS0R4BSE	TEMEX
C7,C8,C9,C10,C11	5	10uF MLCC	GRM32EC72A106ME05	Murata
C5	1	0.2pF High Q Capacitor	251SHS0R2BSE	TEMEX
C12,C13,C14	3	1nF MLCC	GRM2162C2A102JA01D	Murata
R1	1	2.7Ω Power Resistor	ESR03EZPF2R70	ROHM

Package Dimensions （Unit:mm）



Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2022/12/30	Rev 1.0	Product Datasheet
2023/8/17	Rev 1.1	Update the package drawing to be more understandable for soldering

Application data based on LWH-22-13

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