



3W,12.5V High Power RF LDMOS FETs

ITEH25007C6

Description

The ITEH25007C6 is a 3-watt, highly rugged, unmatched LDMOS FET, designed for commercial and industrial applications at frequencies up to 3.5GHz. It can be used in linear or saturated power amplifier, for CW and pulsed signal, and any modulation format. It is also featured by its lower cost of plastic open cavity for surface mount on PCB through vias



- Typical 2.45GHz CW Performance (On Innogrator fixture with device soldered).

V_{ds} = 12.5V, I_{dq} = 45mA

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff (%)	P1dB Gain (dB)	P3dB (dBm)	P3dB (W)	P3dB Eff (%)
2400	34.56	2.9	55.3	16.63	35.51	3.6	59.2
2450	34.03	2.5	55.8	17.66	35.2	3.3	60.0
2500	33.34	2.2	55.8	17.33	34.78	3.0	59.2

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- VHF/UHF Land mobile radio (LMR)
- L band power amplifier
- S band power amplifier
- 12V GaAs transistor replacement

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V _{DSS}	+70	Vdc
Gate--Source Voltage	V _{GS}	-10 to +10	Vdc
Operating Voltage	V _{DD}	+28	Vdc
Storage Temperature Range	T _{stg}	-65 to +150	°C
Case Operating Temperature	T _c	+150	°C
Operating Junction Temperature	T _j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T _c = 85°C, T _j =200°C, DC test	R _{θJC}	5	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)



Characteristic	Symbol	Min	Typ	Max	Unit
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DC Characteristics

Drain-Source Voltage $V_{GS}=0, I_{DS}=100\mu A$	$V_{(BR)DSS}$		70		V
Zero Gate Voltage Drain Leakage Current $(V_{DS} = 13.6V, V_{GS} = 0V)$	I_{DSS}	—	—	1	μA
Gate--Source Leakage Current $(V_{GS} = 9V, V_{DS} = 0V)$	I_{GSS}	—	—	1	μA
Gate Threshold Voltage $(V_{DS} = 12.5V, I_D = 600\mu A)$	$V_{GS(th)}$	—	2	—	V
Gate Quiescent Voltage $(V_{DD} = 12.5V, I_D = 50mA, \text{Measured in Functional Test})$	$V_{GS(Q)}$	—	2.8	—	V

Load Mismatch (In Innogrations Test Fixture, 50 ohm system): $V_{DD} = 12.5Vdc, I_{DQ} = 50mA, f = 1000MHz$

VSWR 10:1 at 3W pulse CW Output Power	No Device Degradation
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Figure 1: Pin Definition (Top View)



Pin No.	Symbol	Description
8,9,10,11	Vgs/RF In	Vgs and RF input
32,33,34,35	Vds/RF out	Vds and RF output
2,5,7,12,13,18,20,23,25,30,31,36	GND	DC/RF Ground
Others	NC	No connection
Package Base	GND	DC/RF Ground.

Reference Circuit of Test Fixture Assembly Diagram
2.45GHz RO4350B 20mils

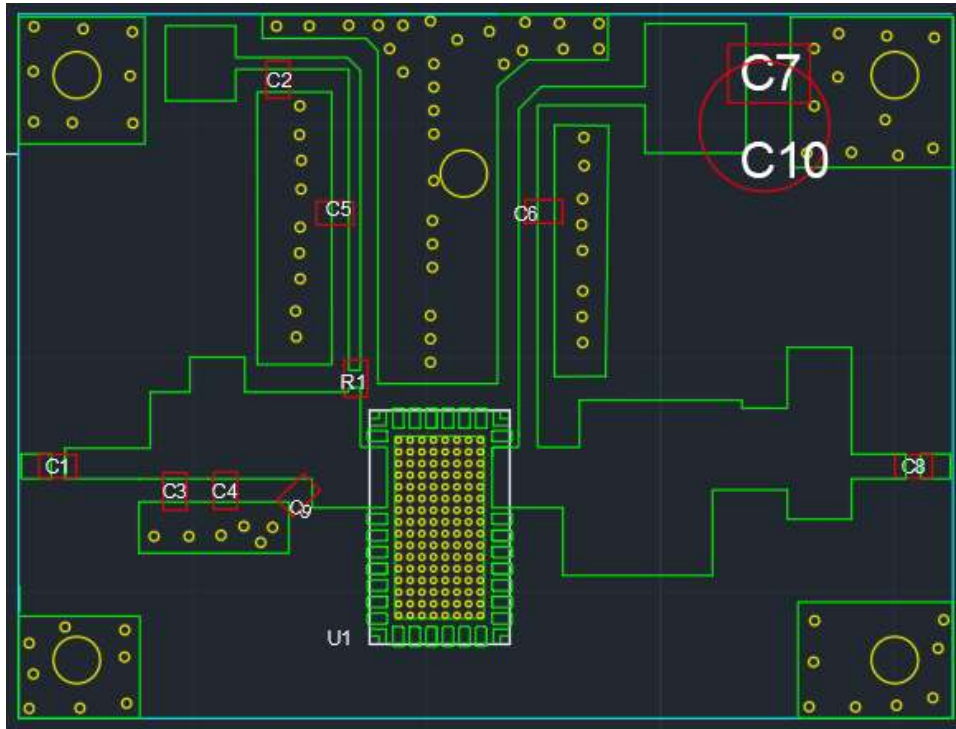


Figure 5. Test Circuit Component Layout

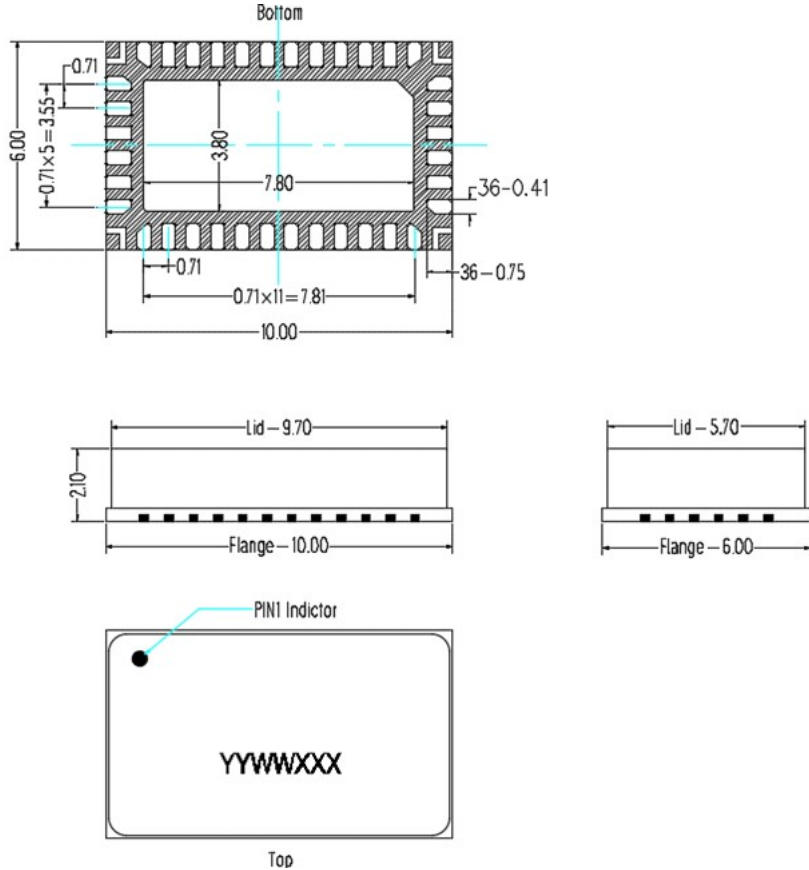
Table 5. Test Circuit Component Designations and Values

BOM		
C2,C7	10uF/63V	ATC600F
C1,C8,C5,C6	20pF	ATC600F
R1	10 ohm	
C9	2.4pF	
C4	0.2pF	
C3	1.1pF	
C10	470uF	



Package Dimensions

10*6 Plastic Package



Notes:

1. All dimensions are in mm;
2. The tolerances unless specified are ± 0.2 mm.

Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2023/6/8	Rev 1.0	Preliminary Datasheet

Application data based on ZXY-23-05

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