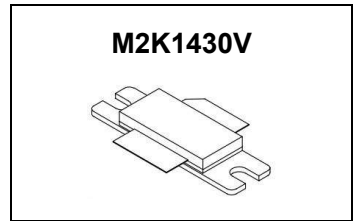


# M2K1430V LDMOS TRANSISTOR

Document Number: M2K1430V  
Preliminary Datasheet V1.0

## 300W, 1.2-1.4GHz 50V High Power RF LDMOS



### Description

The M2K1430V is a 300W single ended 50V LDMOS, internally matched for any applications within 1.2-1.4GHz

It is suitable for use in L band pulsed application especially high duty cycle or wide pulse

It supports any modulated signal at either saturated or linear application.

- Typical performance(on 960-1215MHz application board with devices soldered)

$V_{DS}=50V, I_{dq}=100mA$ , Pulsed CW, **50% duty cycle, 10us pulse width**

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
1200	54.63	290.5	54.5	17.65	55.17	329.1	55.6
1250	54.54	284.7	56.1	17.1	55.07	321.2	56.9
1300	54.4	275.6	55.8	17.1	54.95	312.7	56.6
1350	54.44	278.3	55.7	16.96	54.92	310.5	55.9
1400	54.39	275.0	54.6	16.69	54.84	304.5	54.6

### Features

- High Efficiency and Linear Gain Operations
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Pb-free, RoHS-compliant

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain--Source Voltage	$V_{DSS}$	+115	Vdc
Gate--Source Voltage	$V_{GS}$	-10 to +10	Vdc
Operating Voltage	$V_{DD}$	+55	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature	$T_c$	+150	°C
Operating Junction Temperature	$T_j$	+225	°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case Pulse: Case Temperature 75 °C, 300 W Peak, 10usec Pulse Width, 10% Duty Cycle, 50 Vdc, 1030 MHz	$R_{\theta JC}$	0.2	°C/W

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

**Table 4. Electrical Characteristics** ( $T_A = 25\text{ °C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

### DC Characteristics

# M2K1430V LDMOS TRANSISTOR

Document Number: M2K1430V  
Preliminary Datasheet V1.0

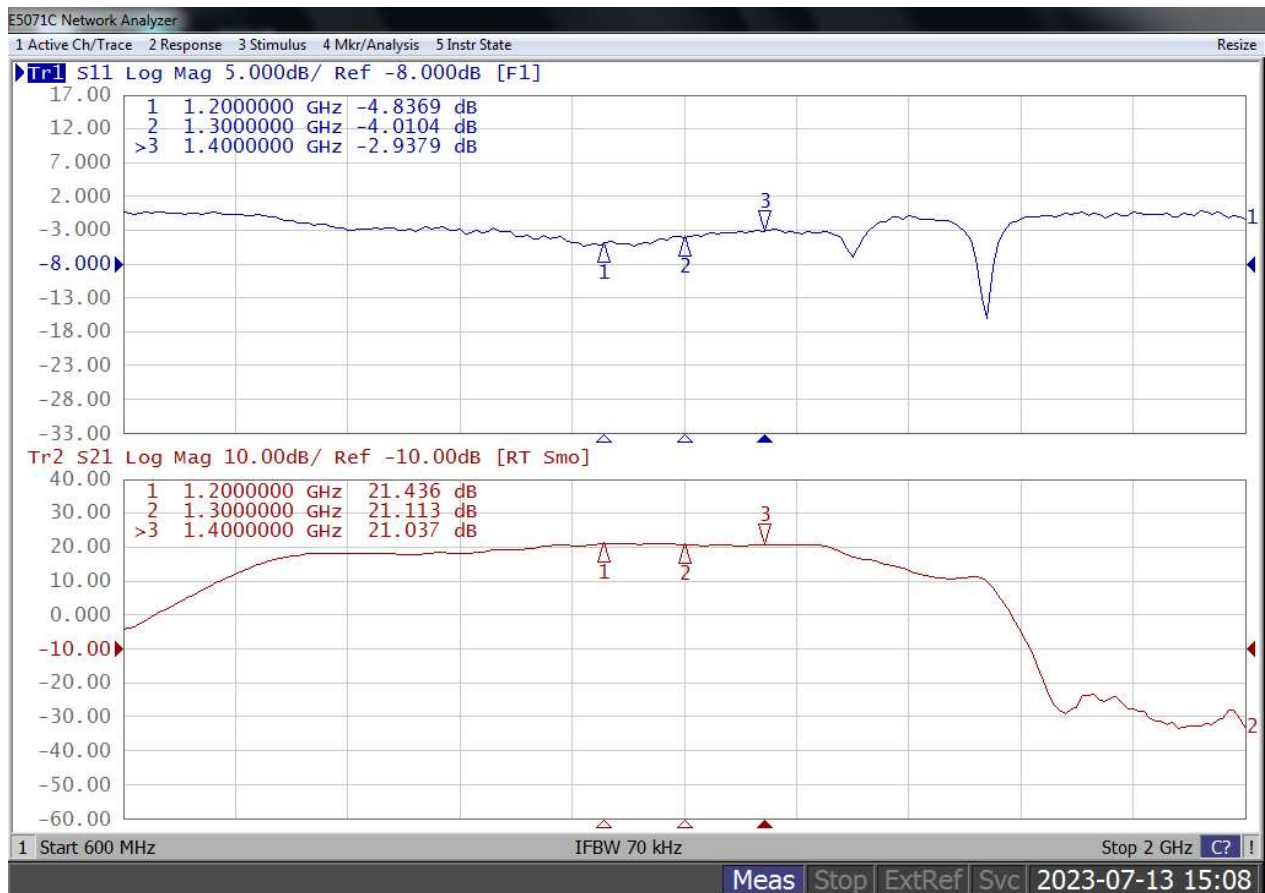
Drain-Source Breakdown Voltage ( $V_{GS}=0V$ ; $I_D=100\mu A$ )	$V_{DSS}$	110			V
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 50 V$ , $V_{GS} = 0 V$ )	$I_{DSS}$			10	$\mu A$
Gate--Source Leakage Current ( $V_{GS} = 6 V$ , $V_{DS} = 0 V$ )	$I_{GSS}$			1	$\mu A$
Gate Threshold Voltage ( $V_{DS} = 50V$ , $I_D = 600 \mu A$ )	$V_{GS(th)}$		1.6		V
Gate Quiescent Voltage ( $V_{DD} = 50 V$ , $I_{DQ} = 100 mA$ , Measured in Functional Test)	$V_{GS(Q)}$		3.1		V

**Load Mismatch (In Innogration Test Fixture, 50 ohm system):**  $V_{DD} = 50 V_{dc}$ ,  $I_{DQ} = 100mA$ ,  $f = 1300MHz$ , pulse width:10us, duty cycle:10%,  $P_{out}=300W$

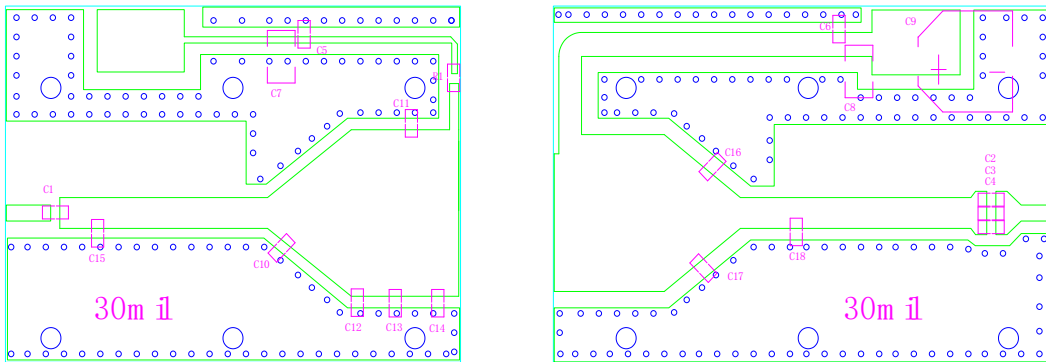
VSWR: > 7:1 at All Phase Angles	No Device Degradation
---------------------------------	-----------------------

## TYPICAL CHARACTERISTICS

Figure 1: Network analyzer output S11/S21 at 50V  $I_{dq}=1500mA$



## Reference Circuit of Test Fixture Assembly Diagram (Layout file upon request, 30mil RO4350)



**Table 5. Test Circuit Component Designations and Values**

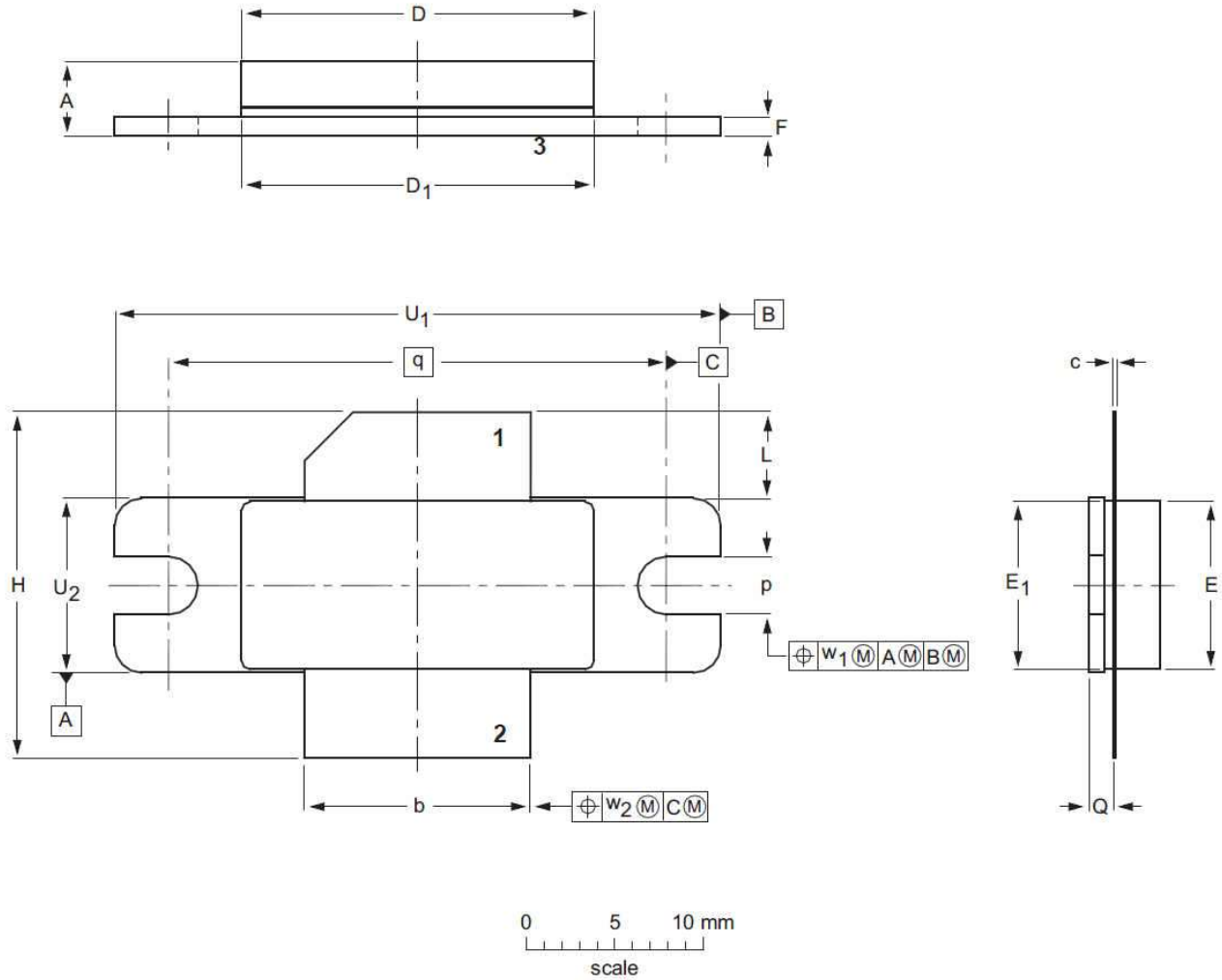
Designator	Comment	Footprint	Quantity
C1, C12	4.7pF/250V	0805	1
C2, C3, C4	20 pF/250V	0805	3
C5, C6	47pF/250V	0805/1210	2
C7, C8	10uF/100V	1210	2
C9	100uF/63V		1
C10, C13, C16, C17	3.3pF/250V	0805	4
C11, C14	6.8pF/250V	0805	1
C15	1.1pF/250V	0805	2
C18	2.2pF/250V	0805	1
R1	10 $\Omega$	0603	1

# M2K1430V LDMOS TRANSISTOR

Document Number: M2K1430V  
Preliminary Datasheet V1.0

## Package Outline

Flanged ceramic package; 2 mounting holes; 2 leads (1—DRAIN, 2—GATE, 3—SOURCE)



UNIT	A	b	c	D	D <sub>1</sub>	E	E <sub>1</sub>	F	H	L	p	Q	q	U <sub>1</sub>	U <sub>2</sub>	W <sub>1</sub>	W <sub>2</sub>
mm	4.72	12.83	0.15	20.02	19.96	9.50	9.53	1.14	19.94	5.33	3.38	1.70	27.94	34.16	9.91	0.25	0.51
	3.43	12.57	0.08	19.61	19.66	9.30	9.25	0.89	18.92	4.32	3.12	1.45		33.91	9.65		
inches	0.186	0.505	0.006	0.788	0.786	0.374	0.375	0.045	0.785	0.210	0.133	0.067	1.100	1.345	0.390	0.01	0.02
	0.135	0.495	0.003	0.772	0.774	0.366	0.364	0.035	0.745	0.170	0.123	0.057		1.335	0.380		

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B2E					03/12/2013

# M2K1430V LDMOS TRANSISTOR

Document Number: M2K1430V  
Preliminary Datasheet V1.0

## Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2023/7/13	Rev 1.0	Preliminary datasheet

Application data based on LSM-23-23

## Disclaimers

Specifications are subject to change without notice. Innogration believes the information contained within this data sheet to be accurate and reliable. However, no responsibility is assumed by Innogration for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Innogration. Innogration makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose. "Typical" parameters are the average values expected by Innogration in large quantities and are provided for information purposes only. These values can and do vary in different applications and actual performance can vary over time. All operating parameters should be validated by customer's technical experts for each application. Innogration products are not designed, intended or authorized for use as components in applications intended for surgical implant into the body or to support or sustain life, in applications in which the failure of the Innogration product could result in personal injury or death or in applications for planning, construction, maintenance or direct operation of a nuclear facility. For any concerns or questions related to terms or conditions, pls check with Innogration and authorized distributors

Copyright © by Innogration (Suzhou) Co.,Ltd.