

ITGV10320BY4 LDMOS TRANSISTOR

Document Number: ITGV10320BY4
Product Datasheet V1.0

300W, 50V High Power RF LDMOS FETs

Description

The ITGV10320BY4 is a 300-watt capable, high performance, input matched LDMOS FET, designed for UHF band up to 1GHz. It can be used for both CW and pulse application.

It is featured for high power and high ruggedness, low cost, suitable for ISM RF Energy application especially 915MHz etc

- Typical Performance (On Innogration 915MHz fixture with device soldered):

$V_{DS} = 50V$, $I_{dq} = 100mA$

Pulse: 10uS width, 10% duty cycle

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
915	54.75	298.8	68.3	22.29	55.41	347.8	69

CW:

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
915	54.67	293.3	67.2	22.06	55.21	332.1	68

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- On chip RC network enable high stability and ruggedness
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	110	Vdc
Gate--Source Voltage	V_{GS}	-7 to +10	Vdc
Operating Voltage	V_{DD}	+50	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case ,Case Temperature 80°C, 300W CW, 50 Vdc, $I_{DQ} = 100 mA$	$R_{\theta JC}$	0.5	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

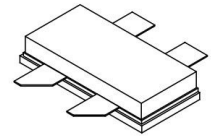
Table 4. Electrical Characteristics ($T_A = 25^\circ C$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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DC Characteristics (Per Side)

Drain-Source Voltage	$V_{(BR)DSS}$	110			V
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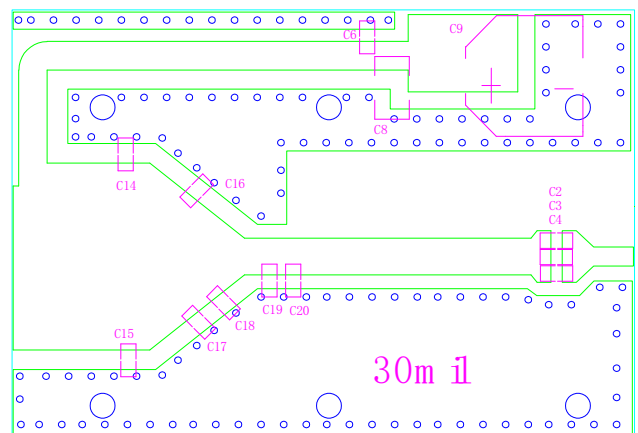
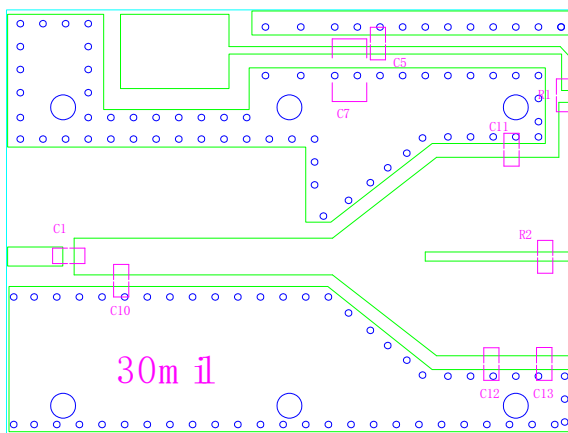


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$V_{GS}=0, I_{DS}=18.0\text{mA}$					
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 50\text{V}, V_{GS} = 0\text{V}$)	I_{DSS}			1	μA
Gate—Source Leakage Current ($V_{GS} = 10\text{V}, V_{DS} = 0\text{V}$)	I_{GSS}			1	μA
Gate Threshold Voltage ($V_{DS} = 50\text{V}, I_D = 600\ \mu\text{A}$)	$V_{GS(th)}$		2.6		V
Gate Quiescent Voltage ($V_{DD} = 50\text{V}, I_D = 100\text{mA}$, Measured in Functional Test)	$V_{GS(Q)}$		3.1		V

Reference Circuit of Test Fixture (915MHz)

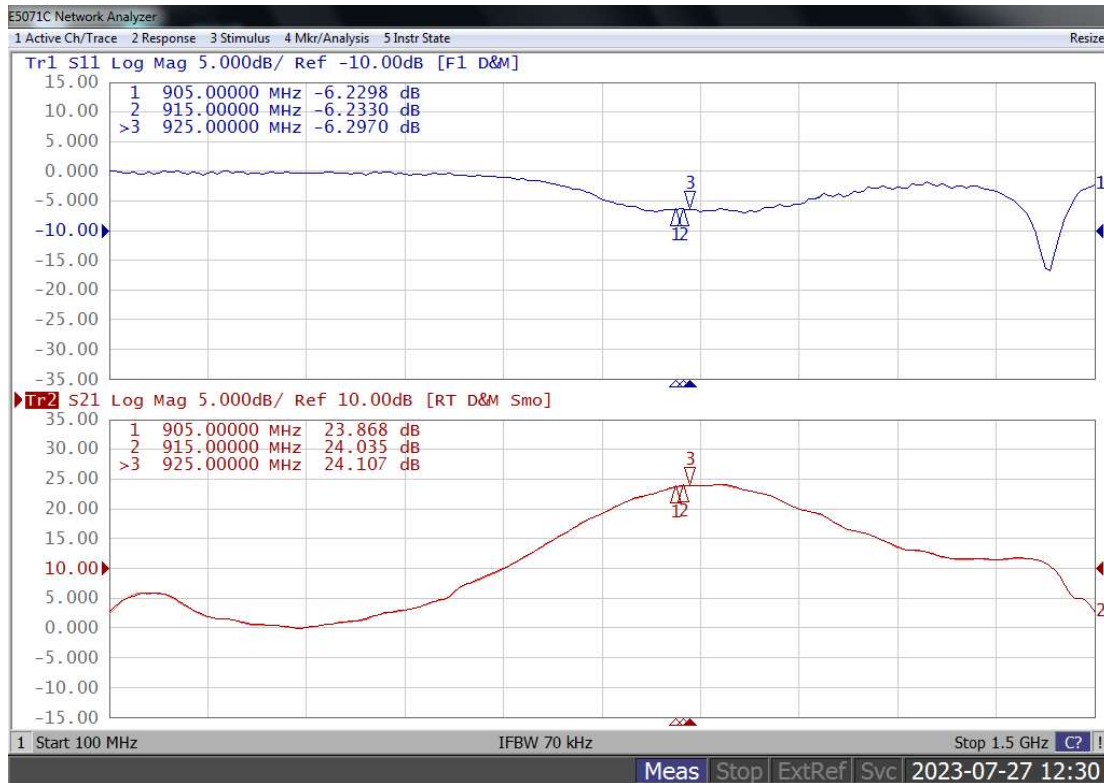


Designator	Comment	Footprint	Quantity
C1, C20	4.7pF/250V	0805	2
C2, C3, C4	20 pF/250V	0805	3
C5, C6	47pF/250V	0805/1210	2
C7, C8	10uF/100V	1210	2
C9	100uF/63V		1
C10	1.1pF/250V	0805	1
C11, C13, C14, C15, C17	6.8pF/250V	0805	5
C12, C16, C18, C19	3.3pF/250V	0805	4
C12, C14	4.7pF/250V	0805	2
R1, R2	10 Ω	0603	2

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Figure 1: Network analyzer output, S11 and S21

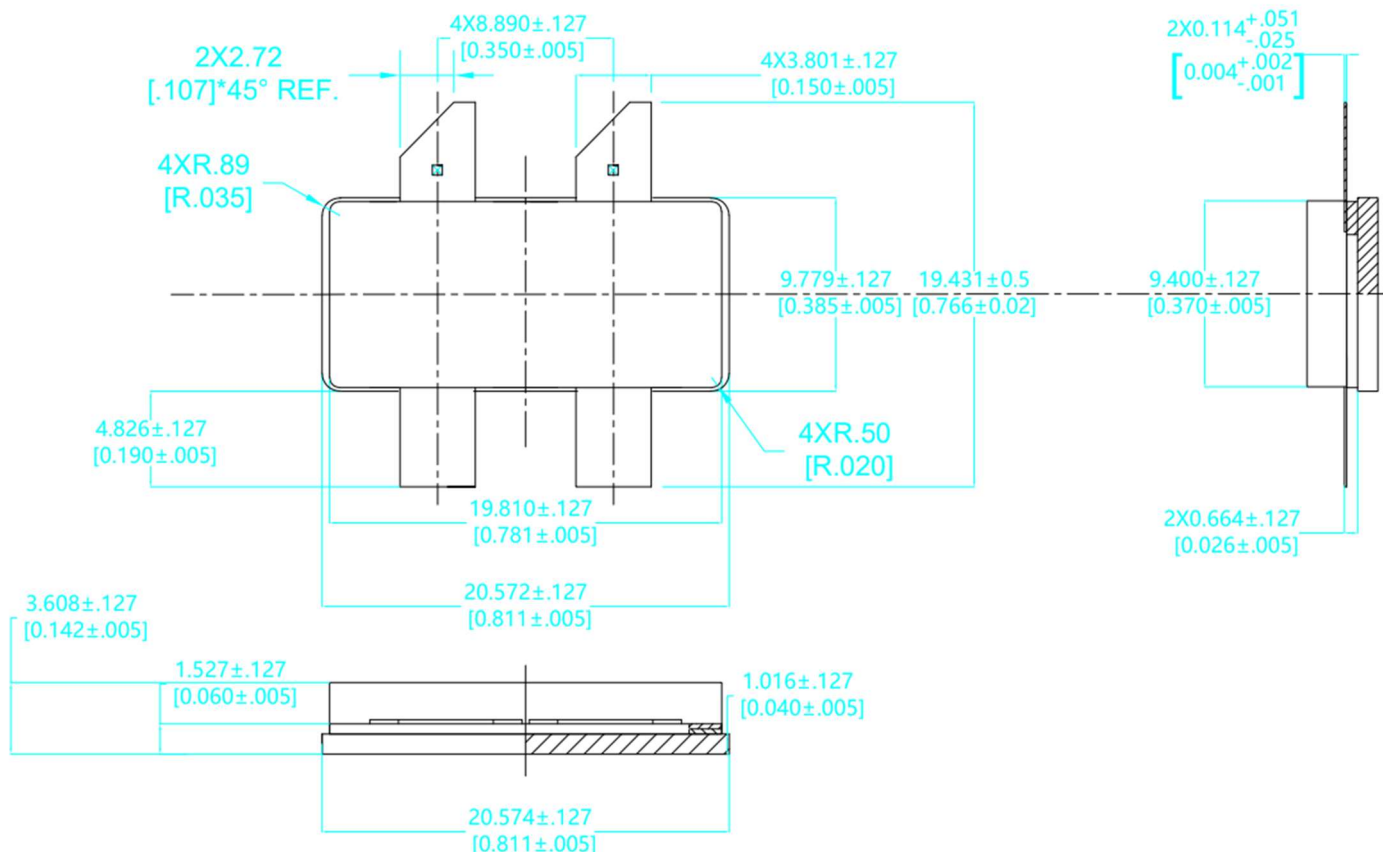


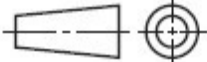
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Package Outline

Earless Flanged Ceramic Package; 4 leads



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-BY4					07/27/2023

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2023/7/27	Rev 1.0	Preliminary Datasheet

Application data based on LSM-23-24

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