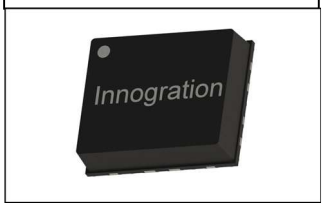
GaN HEMT 50V, 200W,1.8-2.2GHz Full band RF Power Transistor

STBV22W200C9



Description

The STBV22W200C9 is a dual path 200watt, Internally matched GaN HEMT, ideal for applications from 1.8 to 2.2GHz full band operation especially for LTE/5G

There is no guarantee of performance when this part is used outside of stated frequencies.

- Typical RF performance on **1.8-2.2GHz** full band asymmetrical Doherty with device soldered

VDS= 50V, IDQ=200mA(Vgm=-3V，Vgp=-5.3V)

ACPR @45dBm_1C-WCDMA				
Freq (MHz)	Pout (dBm)	ACPR (dBc)	Gain (dB)	Efficiency (%)
1805	45	-27.84	15.80	58.90
1842.5	45	-29.34	16.01	58.66
1880	45	-30.68	16.04	58.34
2000	45	-33.44	15.87	56.95
2100	45	-31.91	14.99	55.61
2135	45	-30.83	14.76	55.33
2170	45	-29.69	14.43	55.28

(1)1C WCDMA; Signal PAR = 10 dB @ 0.01% Probability on CCDF.

Applications

- Asymmetrical Doherty amplifier within 1.8-2.2GHz full band
- Sub-2GHz power amplifier
- CW or pulsed Amplifier

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

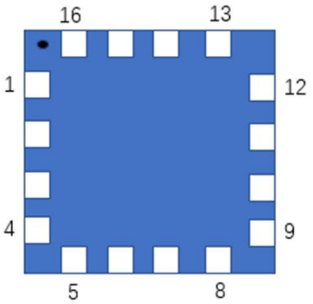
Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically –5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically –5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Pin Configuration and Description （Top view）



Pin No.	Symbol	Description
1,2	RF IN/Vgs of Main	RF Input/Gate bias of main path
3,4	RF IN/Vgs of Peak	RF Input/Gate bias of peak path
9,10	RF OUT/Vds of Peak	RF Output/Drain bias of peak path

11,12	RF OUT/Vds of Main	RF Output/Drain bias of main path
Other Pins	GND	Grounding
Package Base	GND	DC/RF Ground. Proposed to be soldered to heatsink plane directly for the best CW thermal and RF performance. Soldered through vias or copper coin allowed for pulsed CW and back off applications, but will result in higher junction temperatures

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum gate current	Igs	27	mA
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA T_C= 85°C, at Pd=25W, on Doherty application board	$R_{\theta JC}$	2.7	°C /W

Table 3. Electrical Characteristics (TA = 25℃ unless otherwise noted)

DC Characteristics (Main path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=10mA	V_{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 10mA	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	VDS =50V, IDS=100mA, Measured in Functional Test	$V_{GS(Q)}$		-3		V

DC Characteristics (Peak path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=17mA	V_{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 17mA	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	VDS =50V, IDS=150mA, Measured in Functional Test	$V_{GS(Q)}$		-3		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	2.14GHz, Pout=30W WCDMA 1 Carrier in Doherty circuit All phase, No device damages	VSWR		10:1		

Figure 2: Median Lifetime vs. Channel Temperature

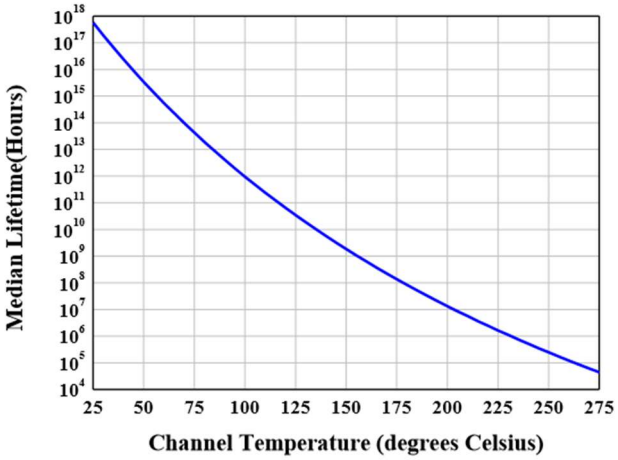
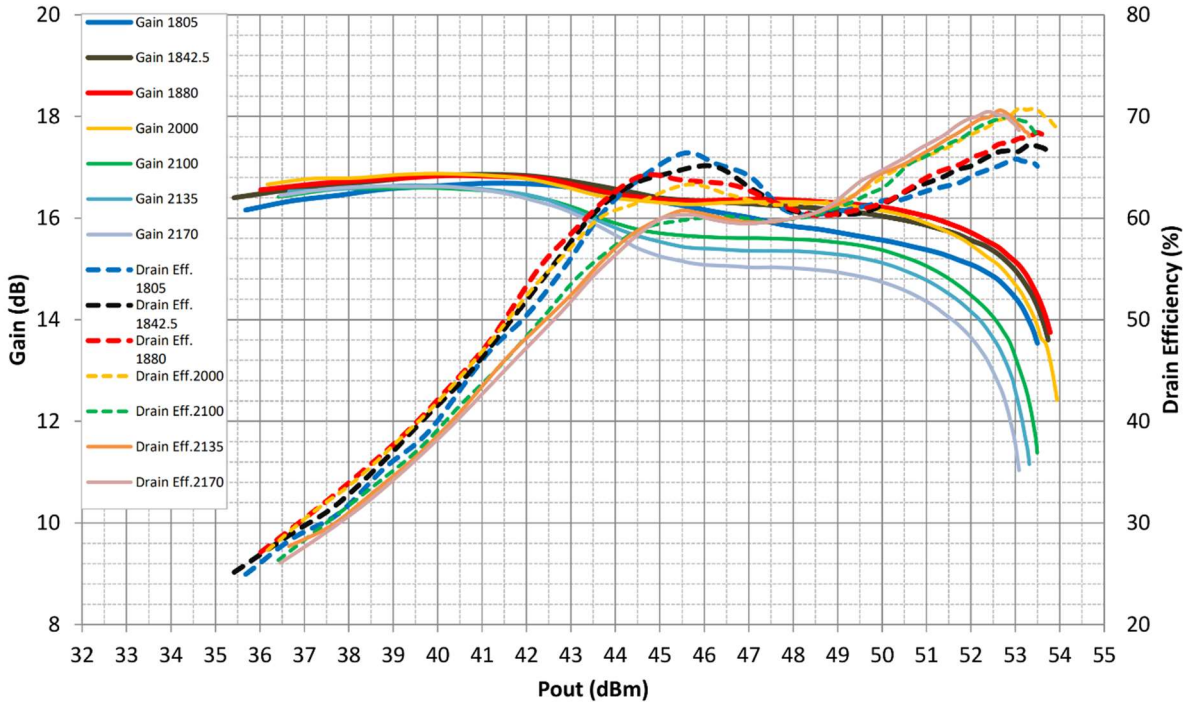


Figure 3: Efficiency and power gain as function of Pout (1.8-2.2GHz Doherty)



Freq (MHz)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)	P4.5dB (dBm)	P4.5dB (W)	P4.5dB Eff(%)
1805	53.49	223.61	65.11	/	/	/
1842.5	53.74	236.63	66.54	/	/	/
1880	53.78	238.94	67.90	/	/	/
2000	53.58	227.93	70.36	53.94	247.58	68.77
2100	52.90	194.99	69.90	53.49	223.45	67.71
2135	52.65	184.27	70.60	53.32	214.58	68.02
2170	52.12	163.10	69.98	53.08	203.47	68.62

Figure 4: Network analyzer output, S11 and S21 (1.8-2.2GHz Doherty)

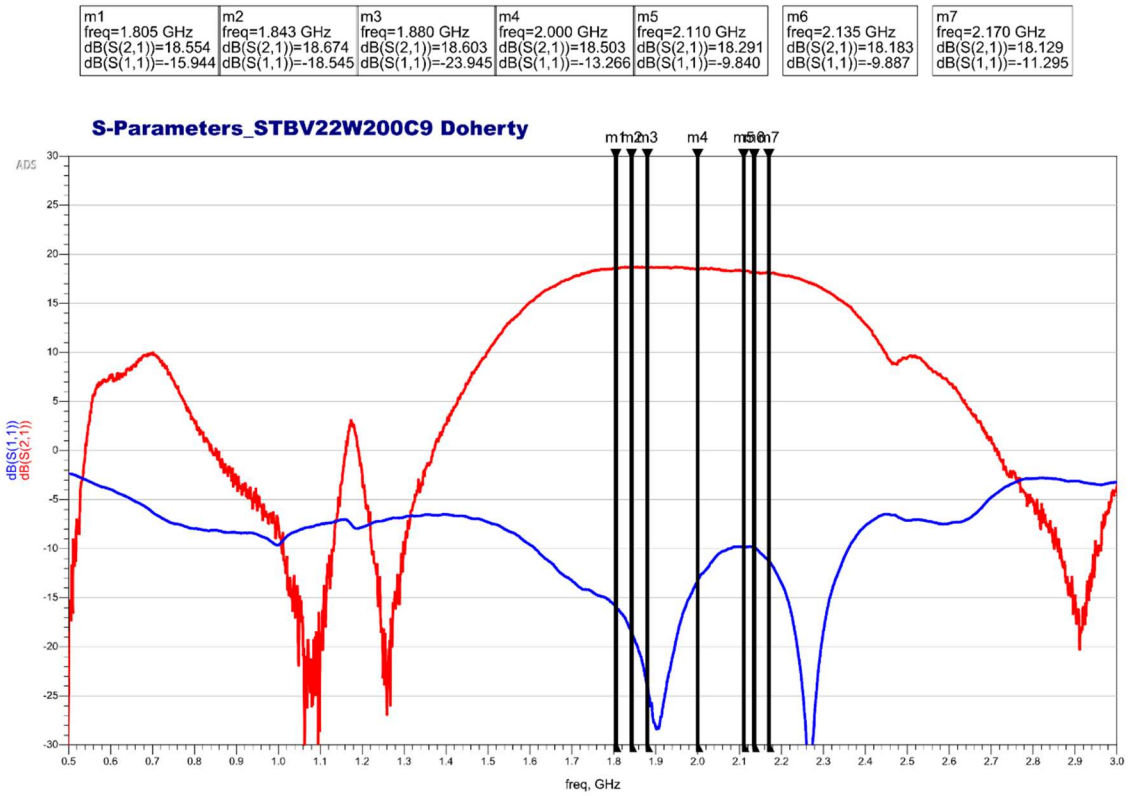


Figure 5: Picture of application board Doherty circuit for 1.8-2.2GHz

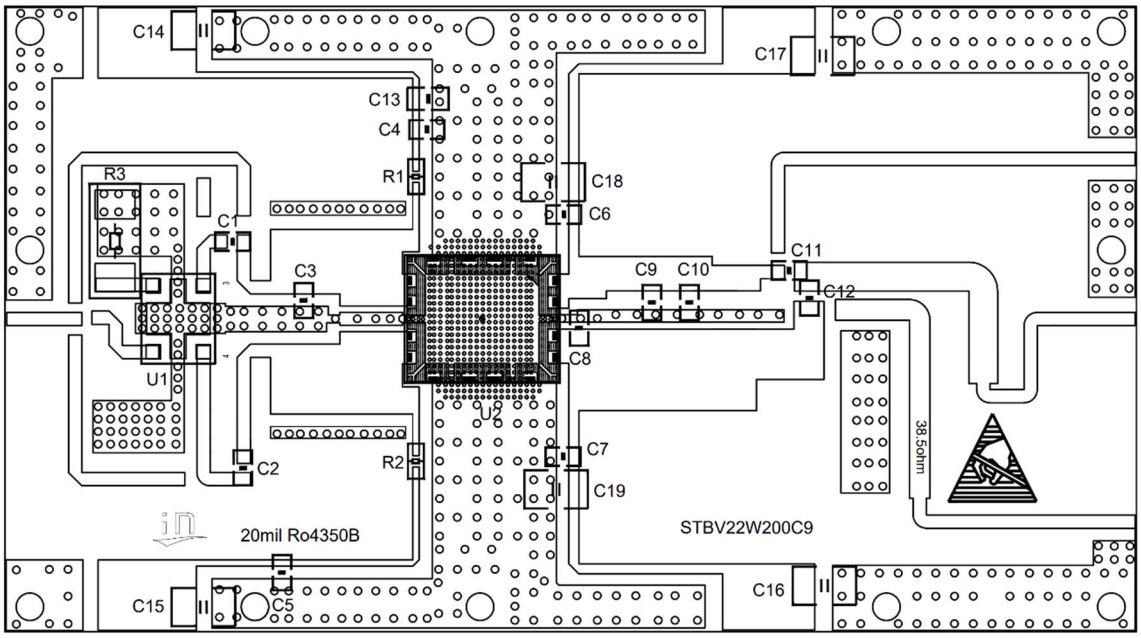
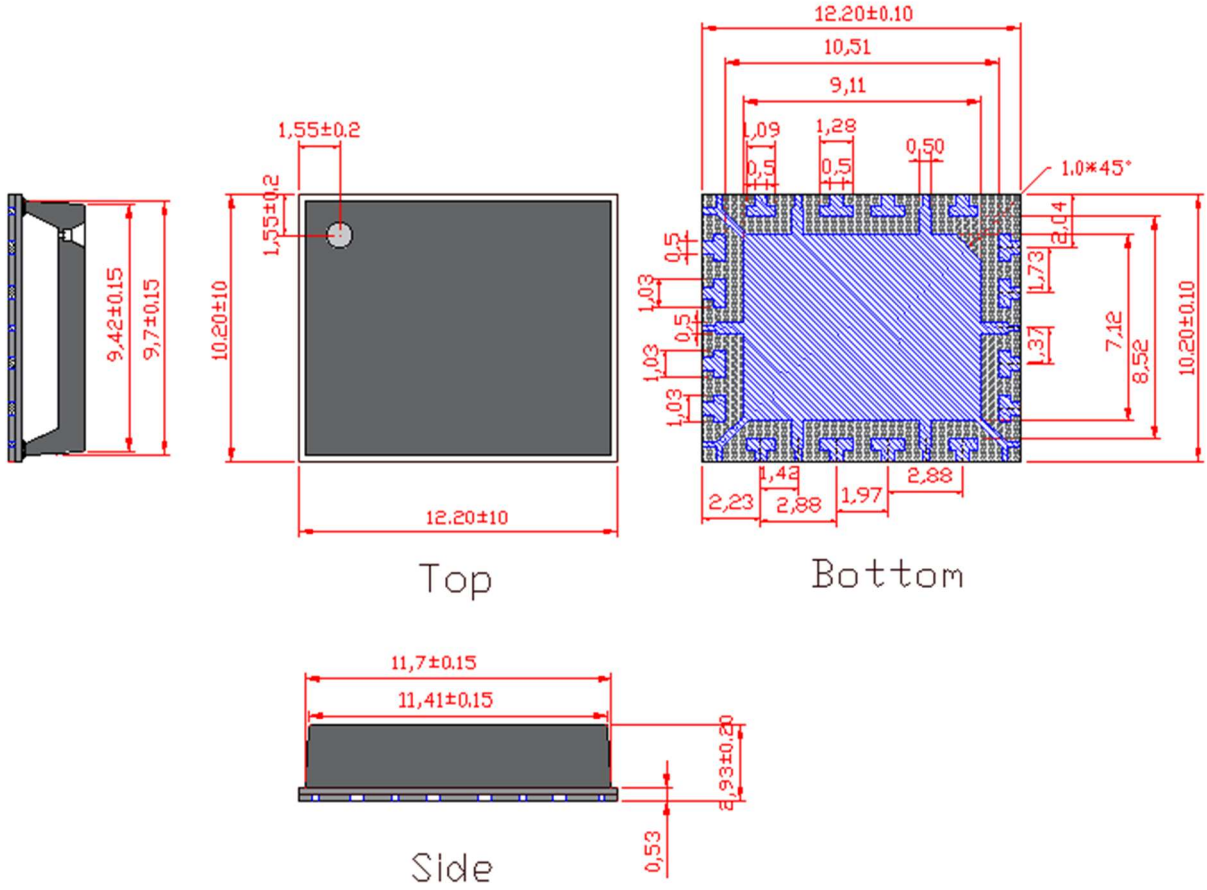


Table 4. Bill of materials of application board (PCB layout upon request, RO4350B 20mils)

Reference	Footprint	Value	Quantity
C1, C2, C4, C5, C6, C7	0603	22pF/250V	6
C3, C9	0603	1.5pF/250V	2
C8	0603	4.7pF/250V	1
C10	0603	1.0pF/250V	1
C11	0603	3.0pF/250V	1
C12	0603	10pF/250V	1
C14, C15, C16, C17, C18, C19	1210	10uF/100V	6
C13	0805	10uF/16V	1
R1, R2	0603	10R	2
R3	2512	51R	1
U1	6.35*5.08mm	HC2100P03H	1
U2	C9	STBV22W200C9^{V1}	1

Package Dimensions （Unit:mm）



Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2023/7/5	V1.0	Preliminary Datasheet Creation
2023/8/17	V1.1	Modification of package drawing on last page
2023/10/25	V1.2	Modify the error of pin definition on 1st page

Application data based on: ZBB-23-31

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