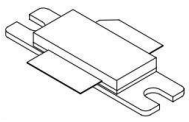
M2K1230V LDMOS TRANSISTOR

Document Number: M2K1230V
Preliminary Datasheet V1.0

300W, 0.96-1.2GHz 50V High Power RF LDMOS

M2K1230V



Description

The M2K1230V is a 300W single ended 50V LDMOS, internally matched for any applications within 0.96-1.215GHz

It is suitable for use in avionics application especially high duty cycle or wide pulse

It supports any modulated signal at either saturated or linear application.

- Typical performance(on 960-1215MHz application board with devices soldered)

V_{DS}=50V,Idq=100mA, Pulsed CW, **50% duty cycle, 10us pulse width**

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
960	54.99	315.8	54.9	18.22	55.65	367.1	57.5
1030	54.98	315.0	58.8	18.47	55.58	361.6	60.8
1090	54.89	308.4	59.8	18.43	55.51	355.4	61.6
1130	54.84	304.9	60.6	19.46	55.39	345.9	61.5
1170	54.75	298.5	59.4	18.69	55.27	336.5	60.2
1215	54.56	286.0	57.0	19.59	55.12	325.5	57.9

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+115	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case Pulse: Case Temperature 75 C, 300 W Peak, 10usec Pulse Width, 10% Duty Cycle, 50 Vdc, 1030 MHz	$R_{\theta JC}$	0.2	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (T_A = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit

DC Characteristics

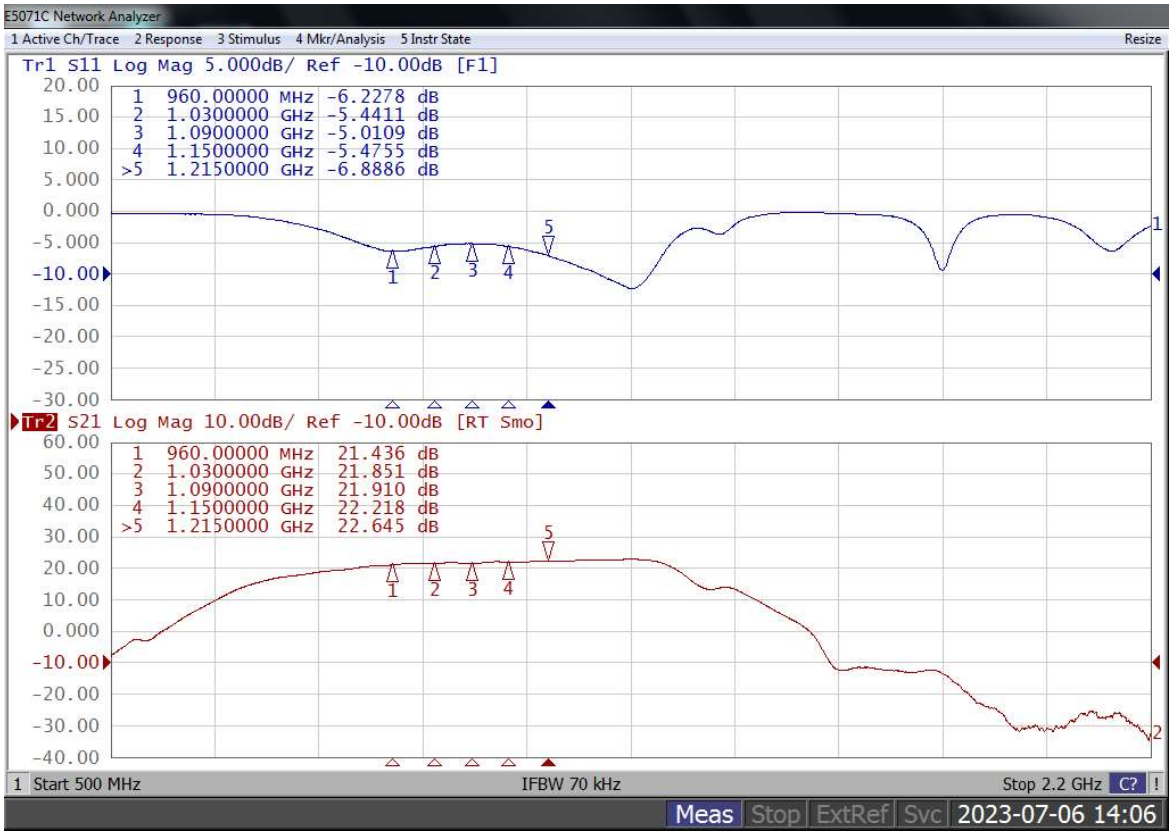
Drain-Source Breakdown Voltage (V_{GS}=0V; I_D=100uA)	V_{DSS}	110			V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50 V, V_{GS} = 0 V)	I_{DSS}			10	μA
Gate--Source Leakage Current (V_{GS} = 6 V, V_{DS} = 0 V)	I_{GSS}			1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 uA)	$V_{GS(th)}$		1.6		V
Gate Quiescent Voltage (V_{DD} = 50 V, I_{DQ} = 100 mA, Measured in Functional Test)	$V_{GS(Q)}$		3.1		V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 50 Vdc, I_{DQ} = 100mA, f = 1030MHz, pulse width:10us, duty cycle:10%, Pout=300W

VSWR: > 7:1 at All Phase Angles	No Device Degradation

TYPICAL CHARACTERISTICS

Figure 1: Network analyzer output S11/S21 at 50V Idq=1500mA



Reference Circuit of Test Fixture Assembly Diagram

(Layout file upon request, 30mil RO4350)

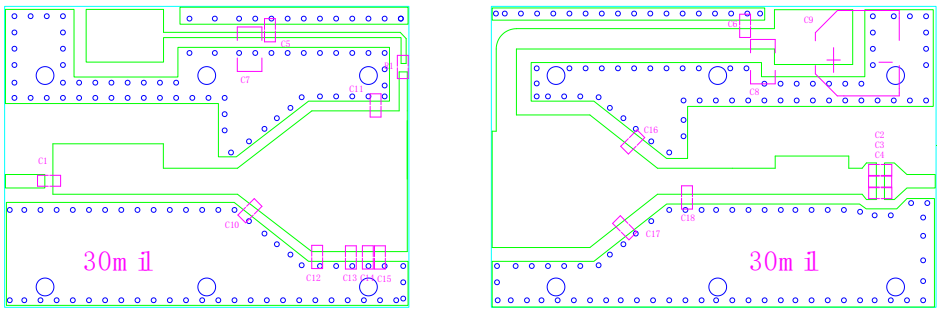
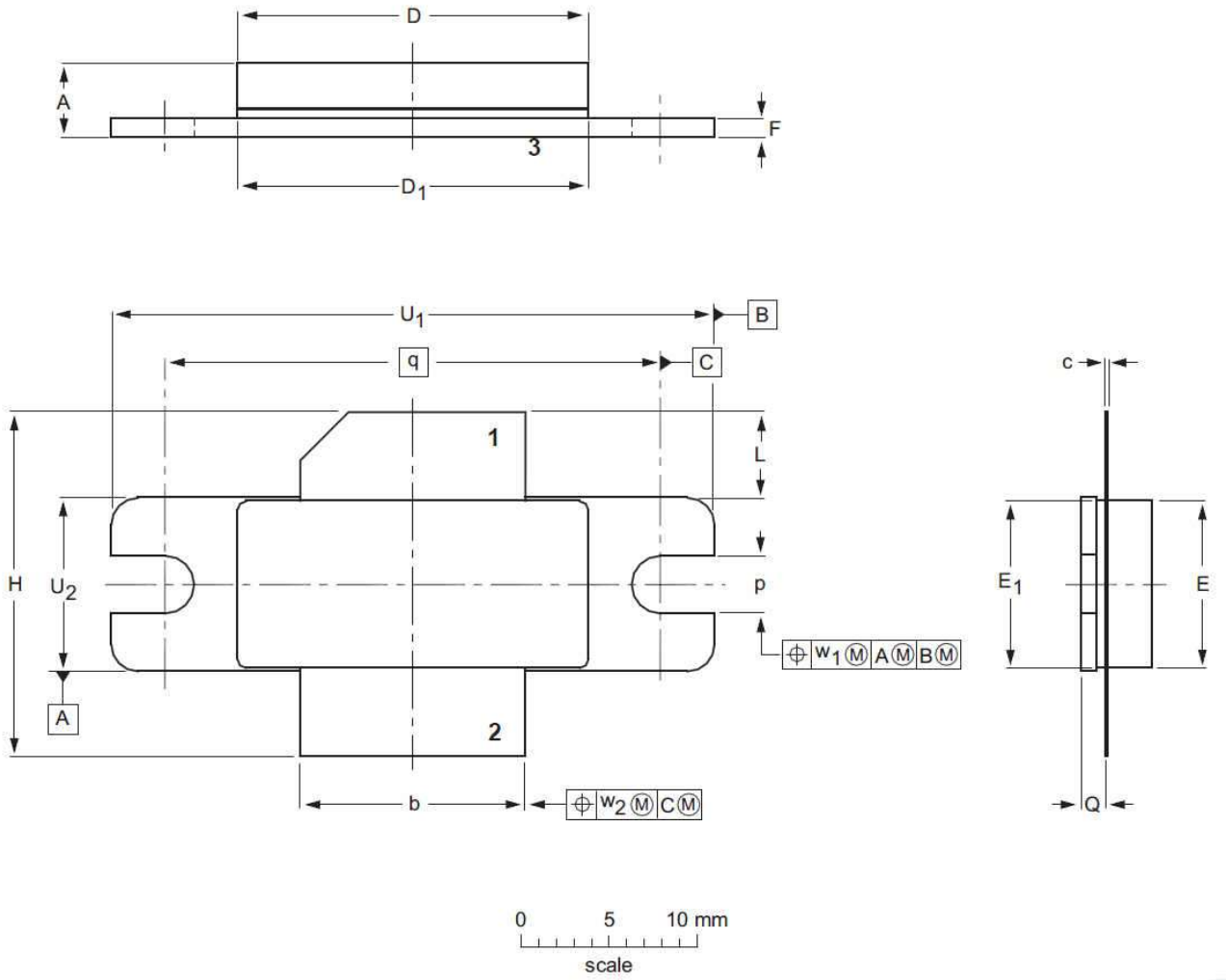


Table 5. Test Circuit Component Designations and Values

Designator	Comment	Footprint	Quantity
C1,	47pF/250V	0805	1
C2, C3, C4	20 pF/250V	0805	3
C5, C6	47pF/250V	0805/1210	2
C7, C8	10uF/100V	1210	2
C9	100uF/63V		1
C10, C13, C15, C16, C17	3.3pF/250V	0805	5
C11	6.8pF/250V	0805	1
C12, C14	4.7pF/250V	0805	2
C18	2.2pF/250V	0805	1
R1	10 Ω	0603	1

Package Outline

Flanged ceramic package; 2 mounting holes; 2 leads（1—DRAIN、2—GATE、3—SOURCE）



UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	W_1	W_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B2E					03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2023/7/7	Rev 1.0	Preliminary datasheet

Application data based on LSM-23-22

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