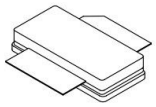
MK2510S LDMOS TRANSISTOR

Document Number: MK2510S
Preliminary Datasheet V2.0

1.8-2.7Hz, 100W, 28V High Power RF LDMOS FETs

MK2510S



Description

The MK2510S is a 100-watt, internally matched LDMOS FETs, designed for wideband applications from 1800 to 2700MHz.

It can be used in Class AB/B and Class C for all pulsed and CW formats.

- Typical Performance (on wideband board with device soldered):

Vds=28V Idq=1A Vgs=3.2V CW

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
1800	49.94	98.7	56.7	12.59	51.24	133.0	62.6
1950	50.48	111.7	59.3	13.71	51.58	143.8	62.7
2100	50.62	115.4	52.9	14.06	51.65	146.2	56.7
2250	50.6	114.7	50.1	14.43	51.57	143.6	53.1
2400	50.63	115.7	50.1	14.33	51.62	145.1	53.3
2550	50.39	109.4	48.4	13.78	51.32	135.4	51.0
2600	49.88	97.4	42.8	13.25	50.88	122.5	45.5
2650	50.28	106.7	46.8	13.6	51.31	135.2	49.9
2700	50.1	102.3	45.0	13.2	51.13	129.7	48.0

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, DC Test	$R_{\theta JC}$	0.55	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Zero Gate Voltage Drain Leakage Current (VDS = 65V, VGS = 0 V)	I_{DSS}			100	μA
Zero Gate Voltage Drain Leakage Current (VDS = 28 V, VGS = 0 V)	I_{DSS}			1	μA
Gate--Source Leakage Current (VGS = 6 V, VDS = 0 V)	I_{GSS}			1	μA
Gate Threshold Voltage (VDS =28V, ID = 300 μA)	$V_{GS(th)}$		2		V
Gate Quiescent Voltage (VDD = 28 V, ID = 1000 mA, Measured in Functional Test)	$V_{GS(Q)}$		3.2		V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28Vdc, I_{DQ} = 100 mA, f = 2200 MHz

VSWR 5:1 at 100W Pulsed CW Output Power	No Device Degradation

TYPICAL CHARACTERISTICS

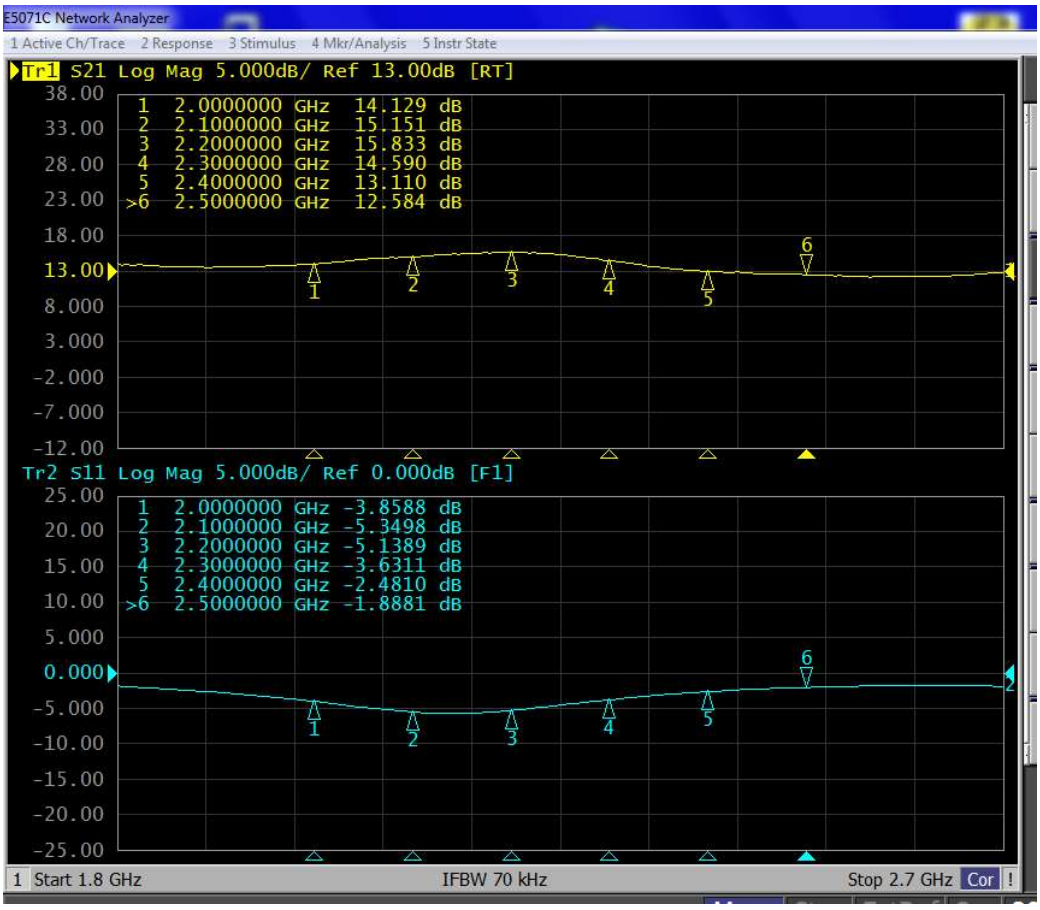
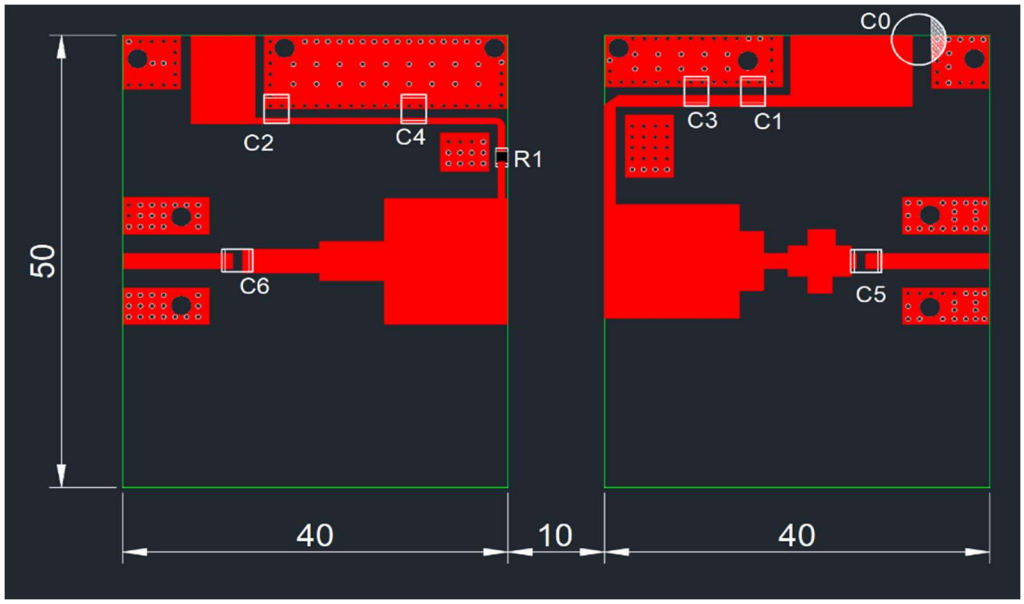


Figure 1. Network analyzer output S11/S21, Idq=1A, Vds=28V

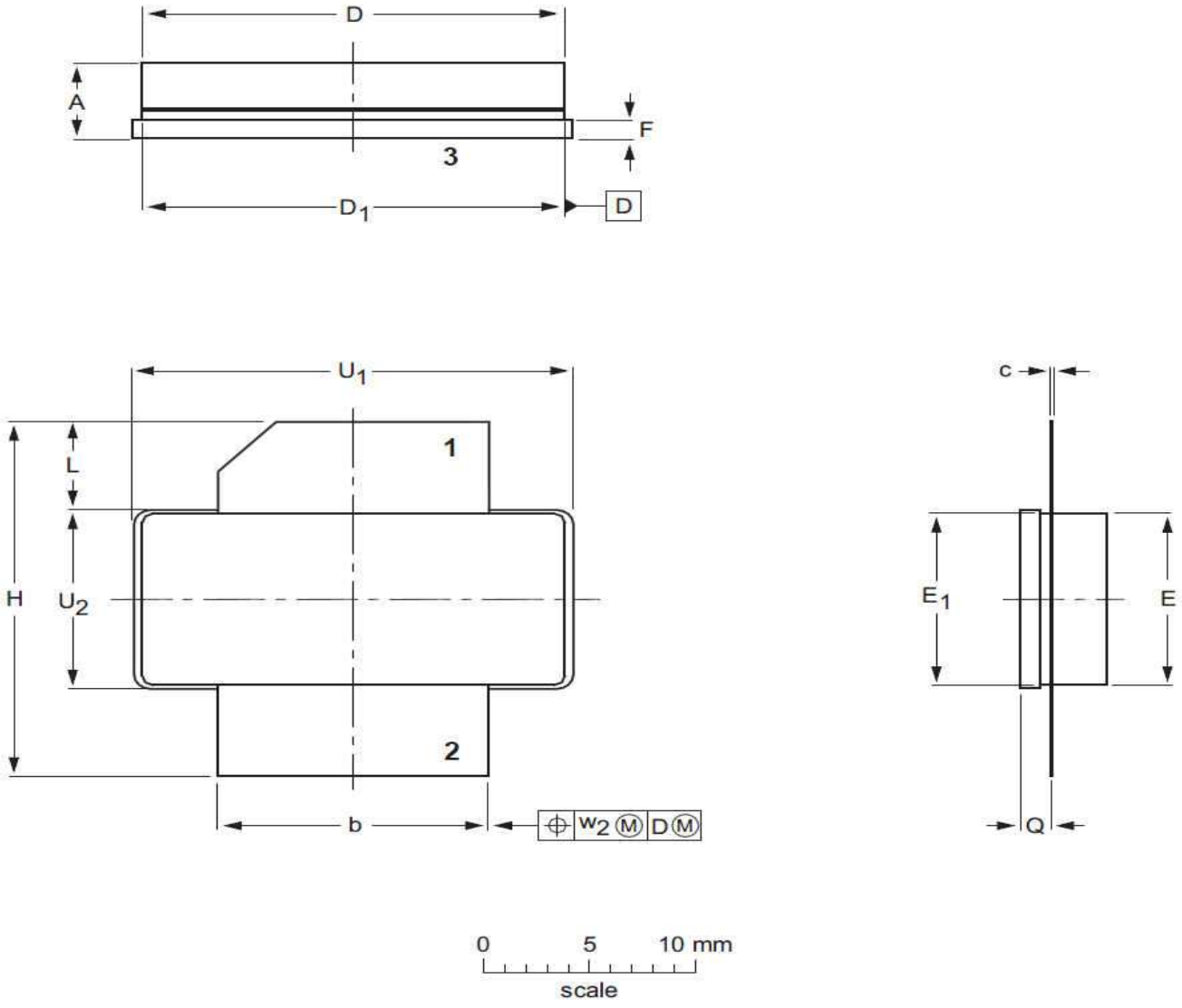
Reference Circuit of Test Fixture Assembly Diagram
(Layout file upon request)



Component	Description	Suggestion
C0	470uF/63V	
C1,C2	10uF	1210
C3,C4,C5,C6	15pF	MQ101111
R1	Chip Resistor,10Ω	0805
PCB	30 Mil Rogers 4350B	

Package Outline

Earless flanged ceramic package; 2 leads



UNIT	A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	W_2
mm	4.72	12.83	0.15	20.02	19.96	9.50	9.53	1.14	19.94	5.33	1.70	20.70	9.91	0.25
	3.43	12.57	0.08	19.61	19.66	9.30	9.25	0.89	18.92	4.32	1.45	20.45	9.65	
inches	0.186	0.505	0.006	0.788	0.786	0.374	0.375	0.045	0.785	0.210	0.067	0.815	0.390	0.010
	0.135	0.495	0.003	0.772	0.774	0.366	0.364	0.035	0.745	0.170	0.057	0.805	0.380	

OUTLINE VERSION	REFERENCE				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
PKG-B2						03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2023/5/15	Rev 1.0	Preliminary Datasheet Creation
2023/7/8	Rev 2.0	Extend the full band support to 1.8-2.7GHz

Application data based on SXY-23-27

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