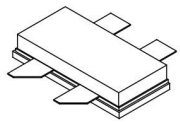
2.4-2.5GHz, 50W*2, Dual path, High Power RF LDMOS FETs

Description

ITCH25100B4



The ITCH25100B4 is a dual path 100W, internally matched LDMOS FETs, designed for multiple use especially RF Energy application including cooking, heating and medical with frequencies from 2400 to 2500MHz.

Each path is 50W capable independently and qualified up to 32V operation.

It is the cost reduction of equivalent 2 pcs of ITCH25050A2

•Typical CW Performance of each path A or B (on Innogration fixture with device soldered):

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
2400	47.77	59.85	58.50	16.52	48.17	65.58	59.56
2450	47.49	56.17	59.28	16.33	47.89	61.49	60.31
2500	46.85	48.43	58.32	16.72	47.45	55.64	59.54

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Figure 1: Pin Connection definition

Transparent top view (Backside grounding for source)

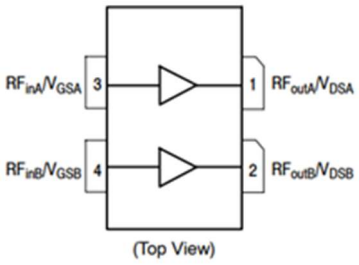


Table 1. Maximum Ratings of each path: A or B

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	65	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics of of each path: A or B

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case Tcase= 85°C, Tj= 200°C, DC Power supply	$R_{\theta JC}$	0.9	°C/W

Table 3. ESD Protection Characteristics of of each path: A or B

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics of each path: A or B (TA = 25 C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Breakdown Voltage (V_{GS}=0V; I_D=100uA)	V_{DSS}	65	——	——	V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	——	——	10	μA
Gate--Source Leakage Current (V_{GS} = 6 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 600 uA)	$V_{GS(th)}$	——	1.75	——	V
Gate Quiescent Voltage (V_{DD} = 28V, I_{DQ} = 100 mA, Measured in Functional Test)	$V_{GS(Q)}$		2.4		V

Load Mismatch (In Innogration Test Fixture, 50 ohm system) of of each path: A or B: V_{DD} = 28 Vdc, I_{DQ} =5 mA, f = 2450MHz

VSWR 10:1 at 50W pulse CW Output Power	No Device Degradation

Figure 1 Efficiency and power gain as function of Pout of each path A or B

Signal: Pulse width 100us, duty cycle 10% , Vgs= 2.24V,Vdd= 28V,Idq=5mA

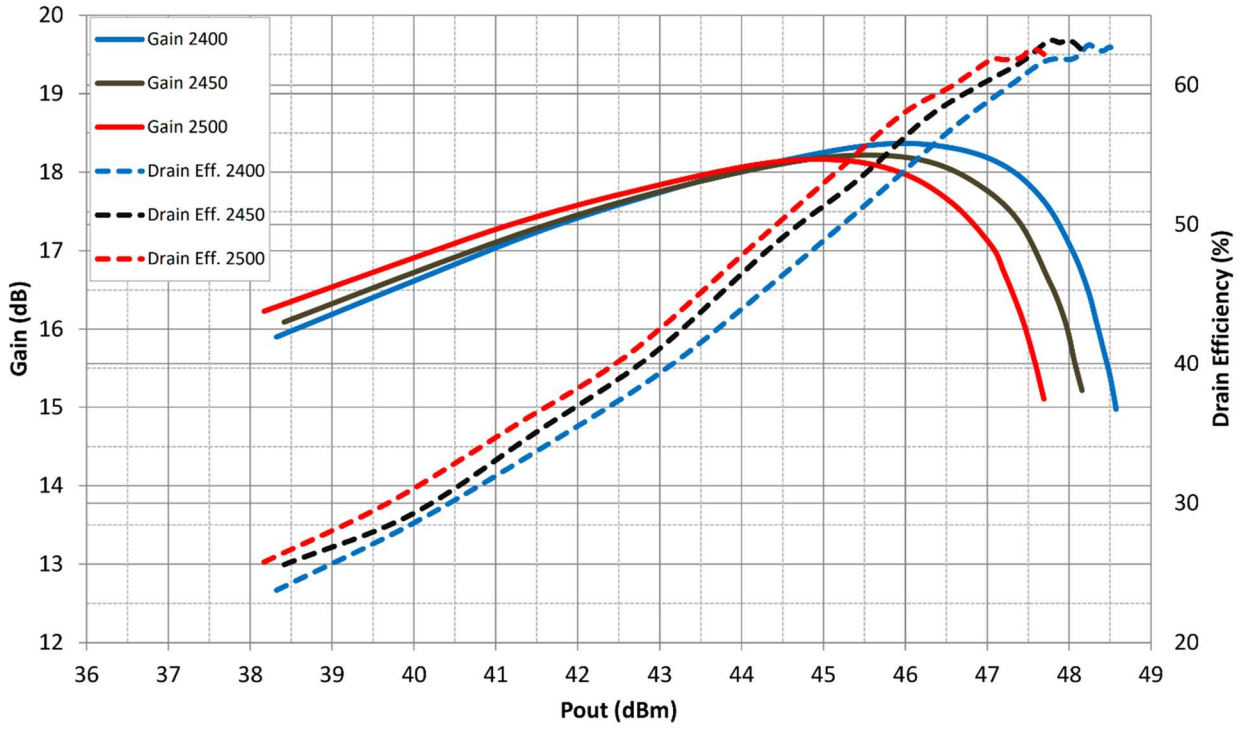


Figure 3: Network analyzer output, S11 and S21

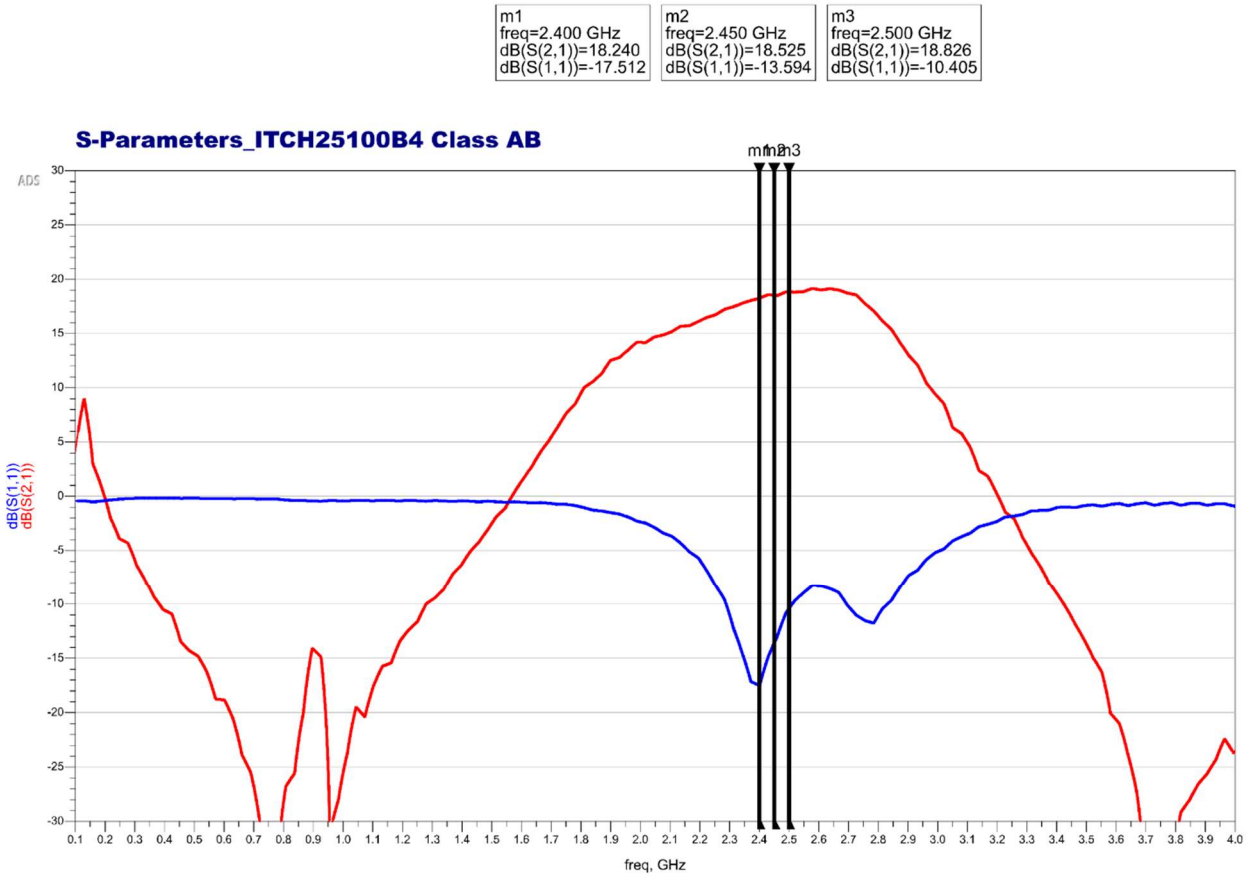


Figure 4: Layout picture (original Gerber file upon request)

Board material: Ro 4350B, Er = 3.48, thickness 20 mils, 1oz copper, unit mm ,

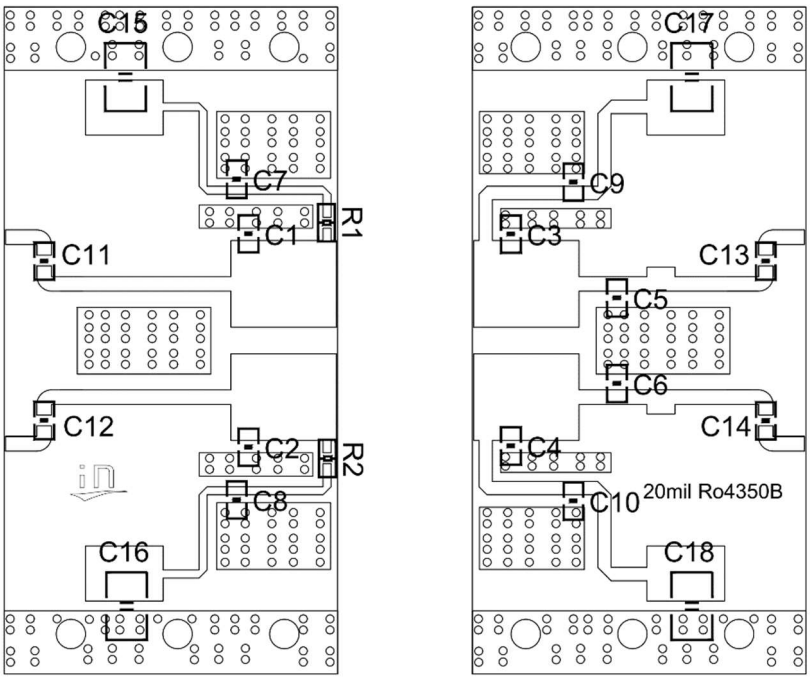
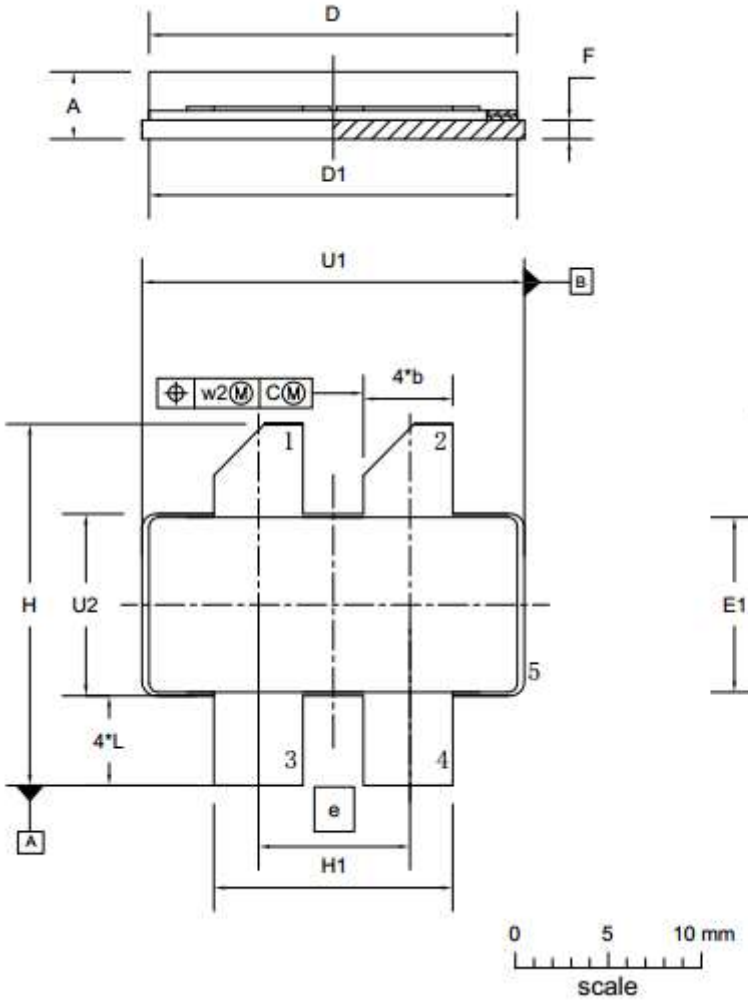


Table 5. List of components

Reference	Footprint	Value	Quantity
C7, C8, C9, C10, C11, C12, C13, C14	0805	12pF/250V	8
C1, C2	0805	1.2pF/250V	2
C3, C4	0805	2.4pF/250V	2
C5, C6	0805	1.0pF/250V	2
C15, C16, C17, C18,	1210	10uF/100V	4
R1, R2	0603	10R	2
/	B4	ITCH25100B4	1

Package Outline

Earless Flanged Ceramic Package; 4 leads



Drain		Gate		Source
1	2	3	4	5

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H1	L	Q	U_1	U_2	W_1	W_2
mm	4.72 3.43	4.67 4.93	0.15 0.08	20.02 19.61	19.96 19.66	7.90	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	12.98 12.73	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25	0.51
inches	0.186 0.135	0.194 0.184	0.006 0.003	0.788 0.772	0.786 0.774	0.311	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.511 0.501	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B4					03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2023/8/10	**V1**	**Preliminary Datasheet Creation**

Application data based on ZBB-23-23

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