GaN 50V, 150W,2.45GHz RF Power Transistor

STBV25150C9

Description

The STBV25150C9 is a single ended 150 watt capable, GaN HEMT, ideal for ISM applications at 2.45GHz. The device offers a more cost effective solution than traditional ceramic device，housed in 12*10mm cost effective plastic open cavity package, and heat dissipated by copper flange directly. There is no guarantee of performance when this part is used outside of stated frequencies.

- Typical RF performance at selected 2.4-2.5GHz applications with device soldered on heatsink

V_{DD} = 48Vdc, Vgs=-3.56V, Idq=1mA

Pulse CW: Pulse width=20us, duty cycle=20%

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
2400	51.51	141.5	71.1	18.75	52.65	184.0	78.3
2450	50.90	123.1	70.9	18.63	52.28	169.0	79.8
2500	50.27	106.5	69.9	18.1	51.8	151.3	80.1

CW:

Freq (MHz)	Pin (dBm)	Power Gain (dB)	Psat (dBm)	Psat (W)	Id (A)	Psat Eff(%)
2400	35.5	16.6	52.15	164	4.60	74.3%
2450	36.5	15.5	52.01	159	4.30	77.0%
2500	37.4	14.4	51.79	151	3.98	79.0%

Applications

- 2.45GHz RF Energy
- S band power amplifier

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

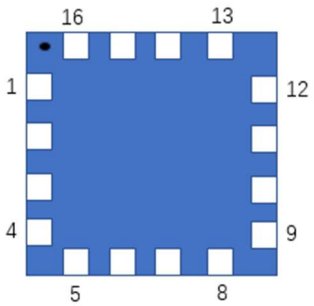
Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically –5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically –5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Pin Configuration and Description （Top view）



Pin No.	Symbol	Description
5-8	RF IN/Vgs	RF Input/Gate bias
13-16	RF OUT/Vds	RF Output/Drain bias
1-4,9-12	NC	Can be left as either no use or grounding
Package Base	GND	DC/RF Ground. Proposed to be soldered to heatsink plane directly for the best CW thermal and RF performance. Soldered through vias or copper coin allowed for pulsed CW applications, but will result in excessive junction temperatures and different RF performance

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum gate current	Igs	21.6	mA
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA T_C= 85°C, at Pd=55W	$R_{\theta JC}$	1.7	°C /W

Table 3. Electrical Characteristics (TA = 25℃ unless otherwise noted)

DC Characteristics (Each path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=21.6mA	V_{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 21.6mA	$V_{GS(th)}$	-4	-	-2	V
Gate Quiescent Voltage	VDS =48V, IDS=190mA, Measured in Functional Test	$V_{GS(Q)}$		--3.0		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	2.45GHz, Pout=150W pulse CW All phase, No device damages	VSWR		10:1		

TYPICAL CHARACTERISTICS

Figure 1: Efficiency and power gain as function of Pout

(V_{DD} = 48Vdc, I_{DQ} = 1mA, Pulse width=20us, duty cycle=20%)

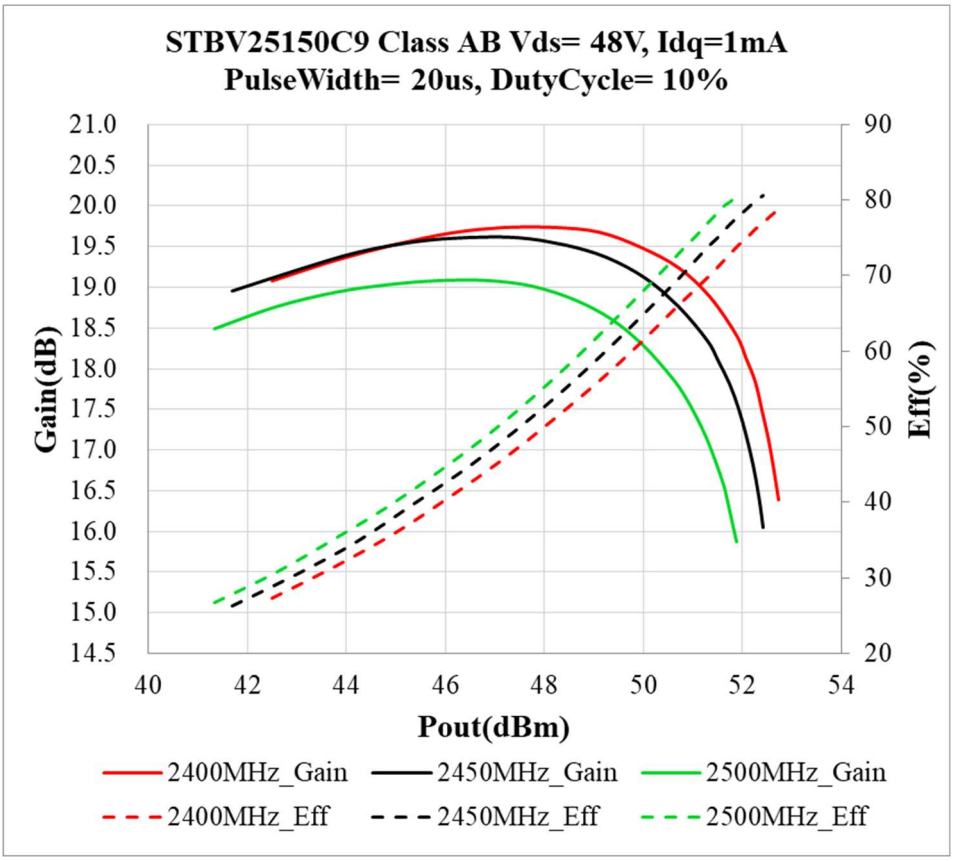


Figure 2: S11/S21 output from Network analyser

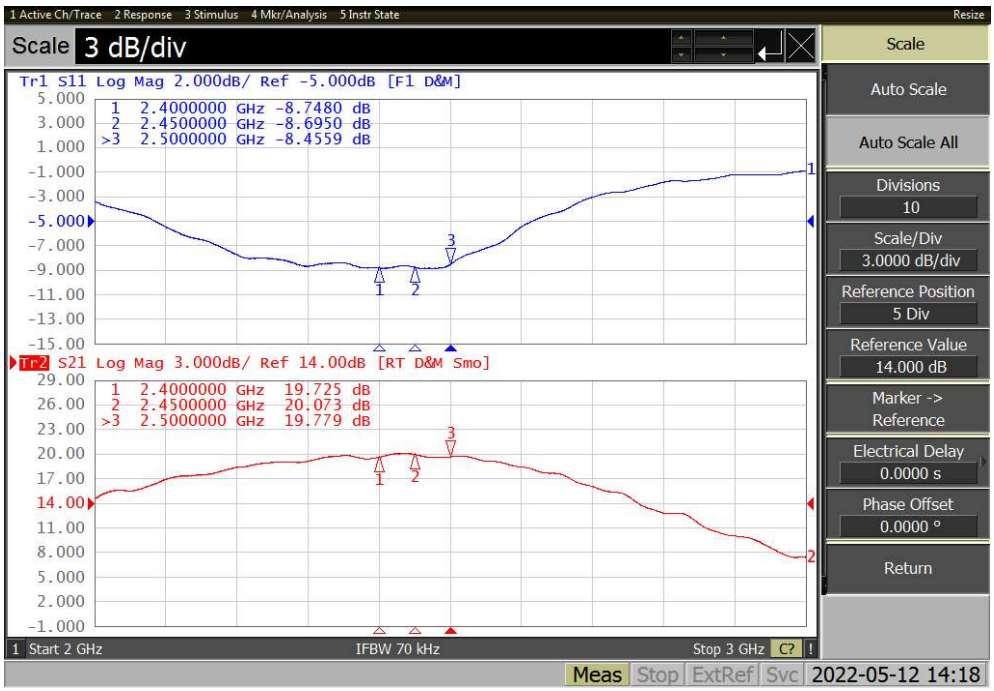
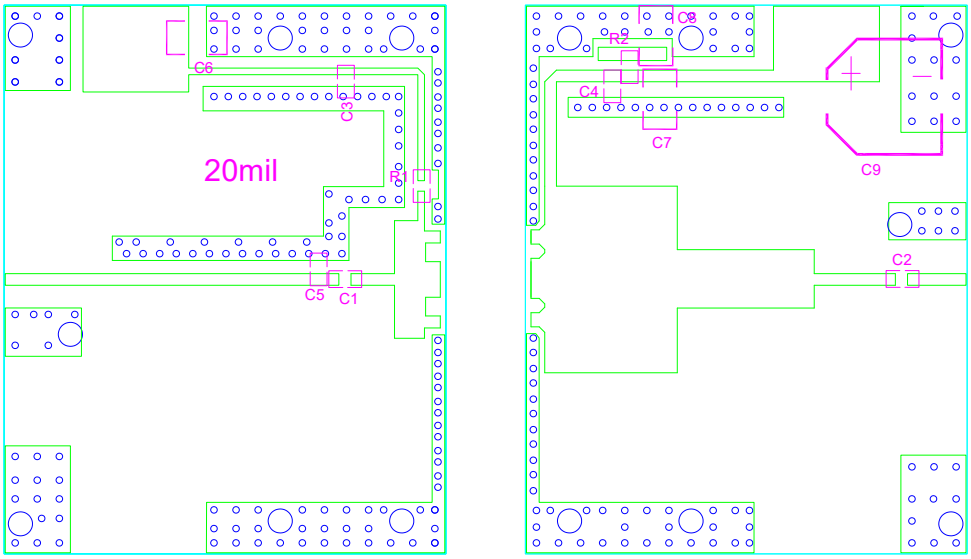
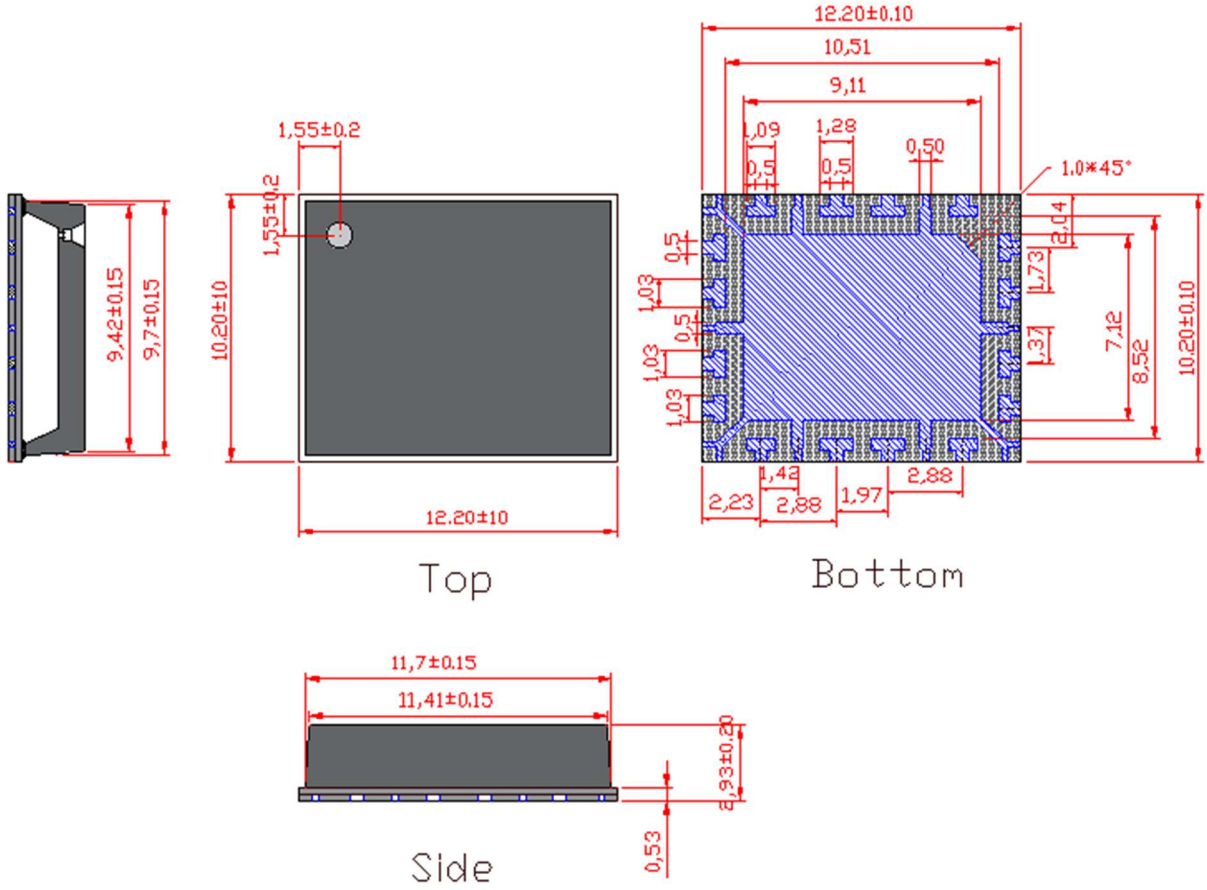


Figure 3: Reference design circuit (RO4350B 20mil, PCB DWG file upon request,)



Designator	Comment	Footprint	Quantity
C1, C2, C3, C4	12 pF	0805	4
C5	1.5 pF	0805	1
C6, C7, C8	10 uF/100V	1210	2
C9	100 uF/63V		1
R1	10 Ω	0603	1
R2	10 Ω	0805	1

Package Dimensions （Unit:mm）



Revision history

Table 1. Document revision history

Date	Revision	Datasheet Status
2022/5/13	Rev 1.0	Preliminary Datasheet
2022/1/31	Rev 1.1	Update the package drawing to be more understandable for soldering

Application data based on LSM-22-07

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