

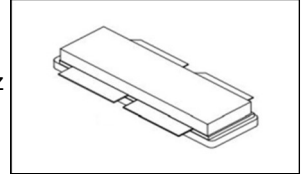


## GaN 50V, 1000W, RF Power Transistor

**STCV131K0RD4**

### Description

The STCV131K0RD4 is a push pull 1000W saturated power capable, internally matched GaN HEMT, ideal for ISM or RF energy applications at fixed frequency point or very narrow band within 1.2 to 1.5GHz. There is no guarantee of performance when this part is used outside of stated frequencies.



- Typical CW performance at 1300MHz applications with transistor soldered on heatsink

STCV131K0RD4 V <sub>ds</sub> =50V V <sub>gs</sub> =3.6V CW						
Freq(MHz)	Pout(dBm)	Pout(W)	I <sub>ds</sub> (A)	Pin(dBm)	Gain(dB)	Eff(%)
1300	60.3	1071.52	28.3	42.9	17.4	75.73
	60	1000.00	27.1	42.05	17.95	73.80
	59.5	891.25	25.5	41.12	18.38	69.90
	58.8	758.58	23.3	40.12	18.68	65.11
	57.9	616.60	21	39.09	18.81	58.72
	57	501.19	18.7	38.08	18.92	53.60
	56	398.11	16.6	37.05	18.95	47.96
	54.9	309.03	14.8	36	18.9	41.76
	53.88	244.34	12.9	34.97	18.91	37.88
	52.86	193.20	11.3	33.93	18.93	34.19
	51.73	148.94	9.9	32.9	18.83	30.09

### Applications

- 1.3/1.5GHz particle linear accelerator
- L band power amplifier
- GPS ground station

### Important Note: Proper Biasing Sequence for GaN HEMT Transistors

#### Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically -5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

#### Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically -5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain--Source Voltage	V <sub>DSS</sub>	+200	Vdc
Gate--Source Voltage	V <sub>GS</sub>	-8 to +0.5	Vdc
Operating Voltage	V <sub>DD</sub>	55	Vdc
Maximum gate current	I <sub>gs</sub>	141	mA
Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C
Case Operating Temperature	T <sub>c</sub>	+150	°C
Operating Junction Temperature	T <sub>J</sub>	+225	°C



**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA $T_c = 25^\circ\text{C}$ , at $P_d = 340\text{W}$	$R_{\theta JC}$	0.4	$^\circ\text{C}/\text{W}$

**Table 3. Electrical Characteristics (TA = 25°C unless otherwise noted)**

**DC Characteristics (Each path, measured on wafer prior to packaging)**

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = -8\text{V}$ ; $I_{DS} = 70.5\text{mA}$	$V_{DSS}$		200		V
Gate Threshold Voltage	$V_{DS} = 10\text{V}$ , $I_D = 70.5\text{mA}$	$V_{GS(th)}$	-4	-	-2	V
Gate Quiescent Voltage	$V_{DS} = 50\text{V}$ , $I_{DS} = 120\text{mA}$ , Measured in Functional Test	$V_{GS(Q)}$		-3.48		V

**Ruggedness Characteristics**

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	1.3GHz, $P_{out} = 1000\text{W}$ pulse CW All phase, No device damages	VSWR		5:1		

## TYPICAL CHARACTERISTICS

**Figure 1: S11/S21 output from Network analyser (VDS= 50V, IDQ=500 mA Vgs =-3.45V)**

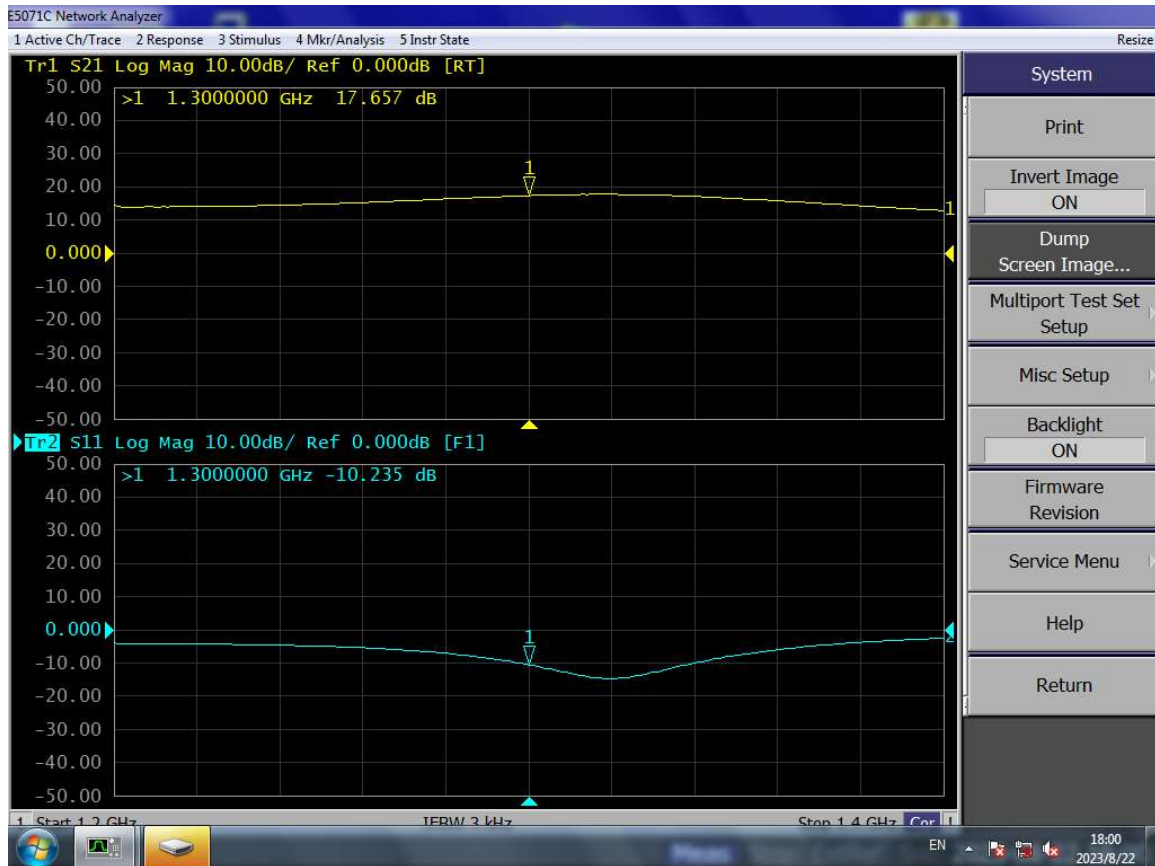
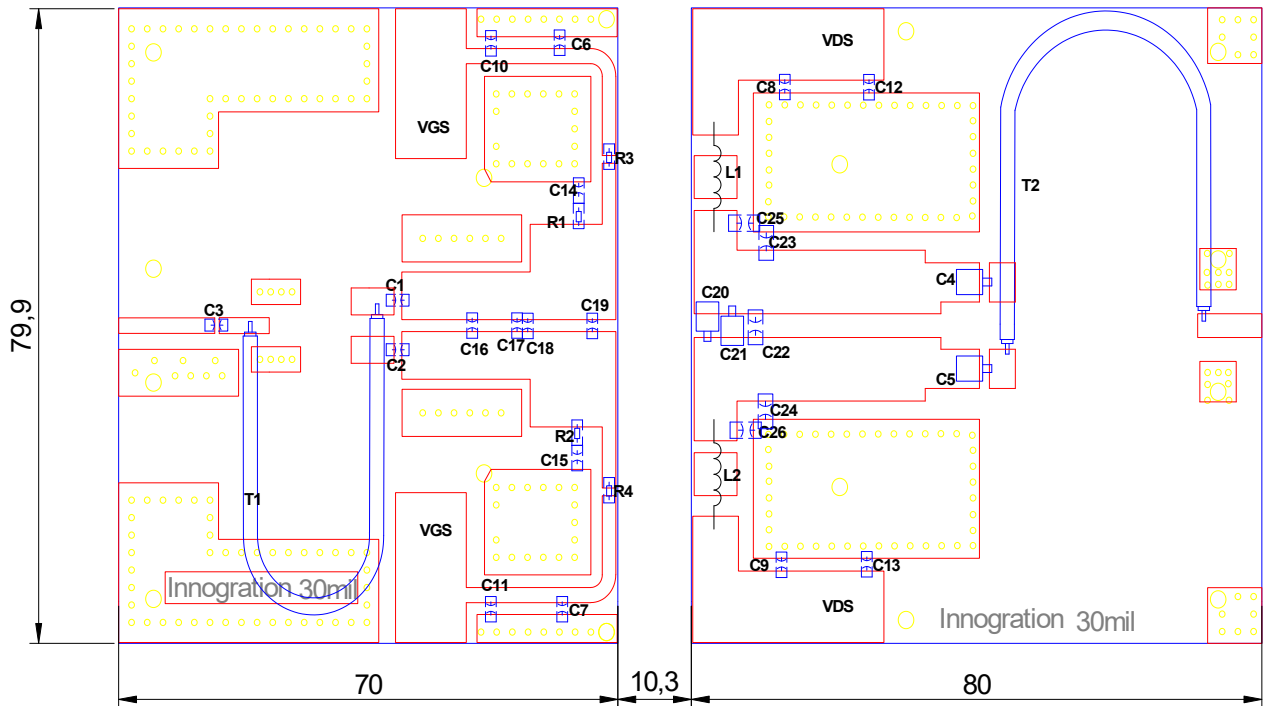


Figure 2: Reference design circuit (PCB DWG file upon request,)

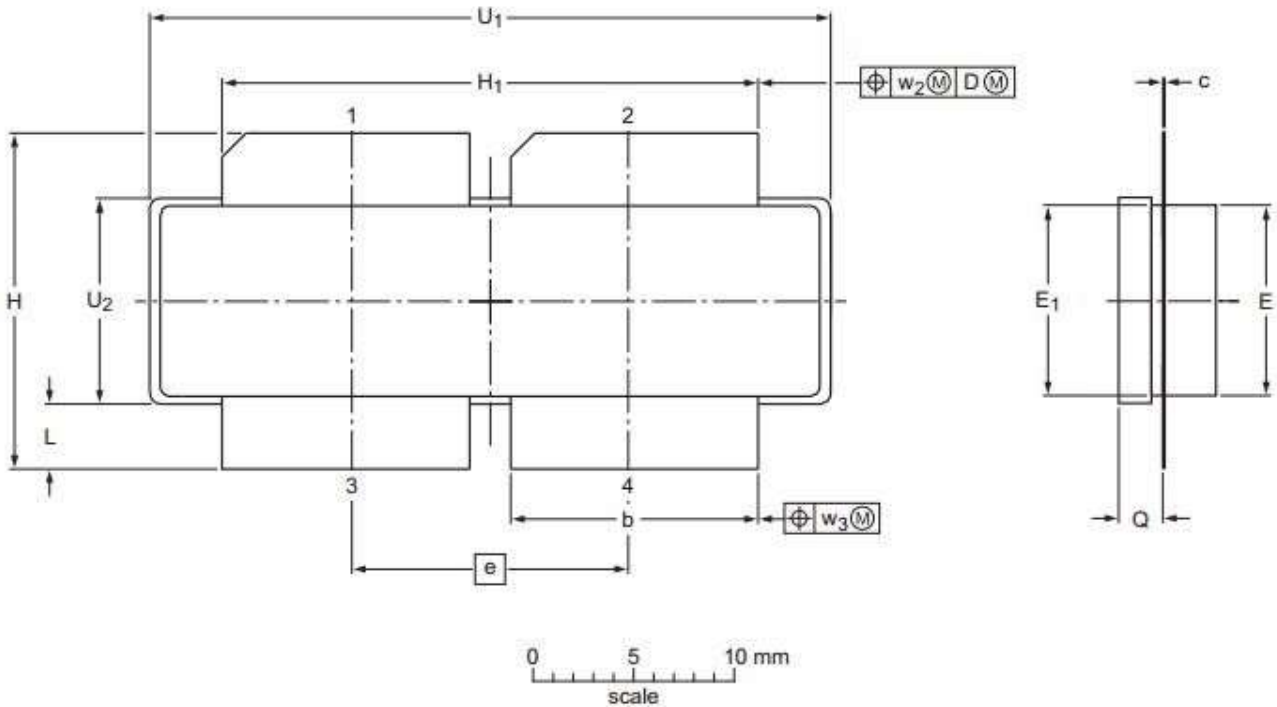
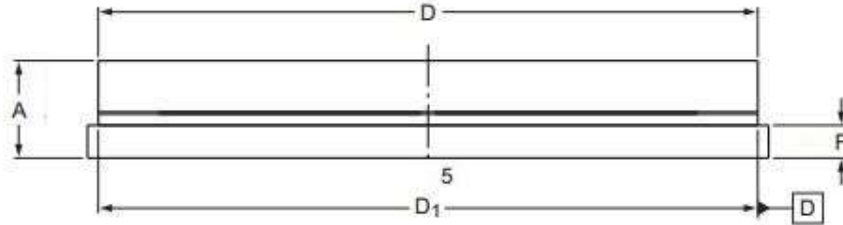


Component	Description	Suggestion
C1,C2,C3	56pF	MQ301111
C4,C5	47pF	Mica capacitance
C6,C7,C8,C9	300pF	10uF/100V
C10,C11,C12,C13,C14,C15	10uF	Ceramic Multilayer Capacitor
C16	2.2pF	MQ301111
C17	3.0pF	MQ301111
C18	1.2pF	MQ301111
C19	4.7pF	MQ301111
C20	4.7pF	Mica capacitance
C21	3.3pF	Mica capacitance
C22	1.8pF	MQ102525
C23,C24	3.6pF	MQ102525
C25,C26	5.1pF	MQ102525
L1,L2	3 Turns, $\phi$ 1.5mm, D=3mm	DIY
R1,R2,R3,R4	10 $\Omega$	Chip Resistor 1026
T1	25ohm,5cm	SFT-25-3
T2	50ohm,6cm	SFT-50-3
PCB	30mil RF-35TC-A	



## Package Outline

Earless flanged ceramic package; 4 leads (1、2—DRAIN、3、4—GATE、5—SOURCE)



UNIT	A	b	c	D	D <sub>1</sub>	e	E	E <sub>1</sub>	F	H	H <sub>1</sub>	L	Q	U <sub>1</sub>	U <sub>2</sub>	W <sub>2</sub>	W <sub>2</sub>
mm	4.7	11.81	0.18	31.55	31.52	13.72	9.50	9.53	1.75	17.12	25.53	3.48	2.26	32.39	10.29	0.25	0.25
	4.2	11.56	0.10	30.94	30.96		9.30	9.27	1.50	16.10	25.27	2.97	2.01	32.13	10.03		
inches	0.185	0.465	0.007	1.242	1.241	0.540	0.374	0.375	0.069	0.674	1.005	0.137	0.089	1.275	0.405	0.01	0.01
	0.165	0.455	0.004	1.218	1.219		0.366	0.365	0.059	0.634	0.995	0.117	0.079	1.265	0.395		

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4					03/12/2013



## Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2022/11/28	V1.0	Preliminary Datasheet Creation
2023/1/7	V1.1	Add 1.3GHz tuned for higher P1dB
2023/3/16	V1.2	Correct T2 info
2023/8/23	V1.3	Update according to the latest application data, only 1.3GHz present

Application data based on: RXT-22-10/HL-23-01

## Notice

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