50W, 28V High Power RF LDMOS FETs

ITDE15050E2

Description

The ITDE15050E2 is a 50-watt, internally matched LDMOS FETs, designed for multiple applications with frequencies from 1 to 1500 MHz.

It can be used in Class AB/B and Class C to support CW,Pulsed CW or any modulation Signal.

•Typical Performance (On Innogration fixture with device soldered) in 3 different bands

VDD = 28 Volts, , CW

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
1470	47.22	52.7	57.6	16.25	48.08	64.3	60.5
1500	46.65	46.3	57.4	16.55	47.69	58.8	60.6
1530	46.27	42.4	57.6	16.31	47.35	54.3	60.3

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
1270	47.15	51.9	60.5	15.95	47.92	62.0	62.8
1300	46.68	46.6	62.2	15.9	47.52	56.5	64.5
1330	46.28	42.4	61.5	16.04	47.13	51.6	62.7

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
885	47.33	54.14	64.31	17.78	48.12	64.92	67.81
915	46.76	47.42	63.83	17.82	47.70	58.94	67.79
945	46.11	40.84	63.24	17.33	47.22	52.70	67.32

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+95	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	1.5	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0, I_{DS}=1.0mA	$V_{(BR)DSS}$	95	——		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 75V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 300 μA)	$V_{GS(th)}$	——	2.15	——	V
Gate Quiescent Voltage (V_{DD} = 28 V, I_D = 100 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.0	——	V
Functional Tests (In Demo Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 130mA, f = 1500 MHz, Pulse Width =10us, Duty Cycle =10%..					
Power Gain	G_p	——	14	——	dB
Drain Efficiency@P3dB	η_D	——	60	——	%
3 dB Compression Point	P_{-3dB}	——	50	——	W
Input Return Loss	IRL	——	-5	——	dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 28 Vdc, I_{DQ} = 130 mA, f = 1500 MHz

VSWR 10:1 at 50W pulse CW Output Power	No Device Degradation

1.5GHz application board

Reference Circuit of Test Fixture Assembly Diagram
20mils RO4350B

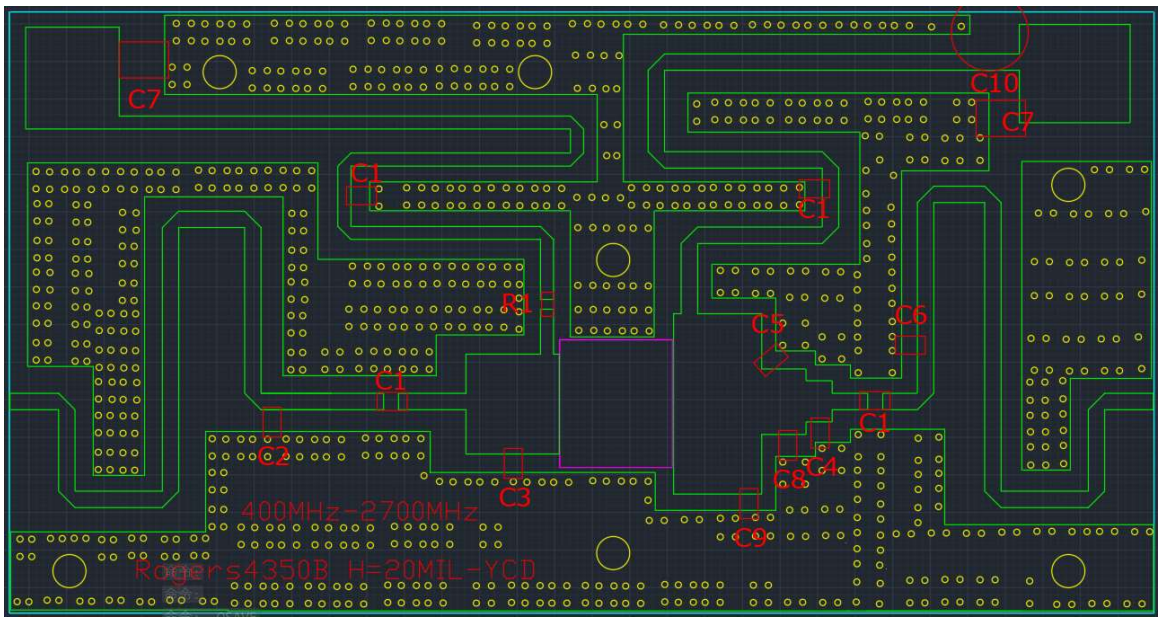


Figure 2. Test Circuit Component Layout

Table 5. Test Circuit Component Designations and Values

Component	Value	Quantity
U1	ITDE15050E2	1
C1	30pF	4
C7	10uF/63V	3
R1	10 Ω	1
C10	470uF/63V	1
C3	4.7pF	1
C9	1.1 pF	1
C2	1.5pF	1
C8	1.8pF	1
C5	5.6pF	1
C4	2.4pF	1
C6	2.2pF	1

TYPICAL CHARACTERISTICS

Figure 3. Power Gain and Drain Efficiency as function of Power Output at Idq =150mA

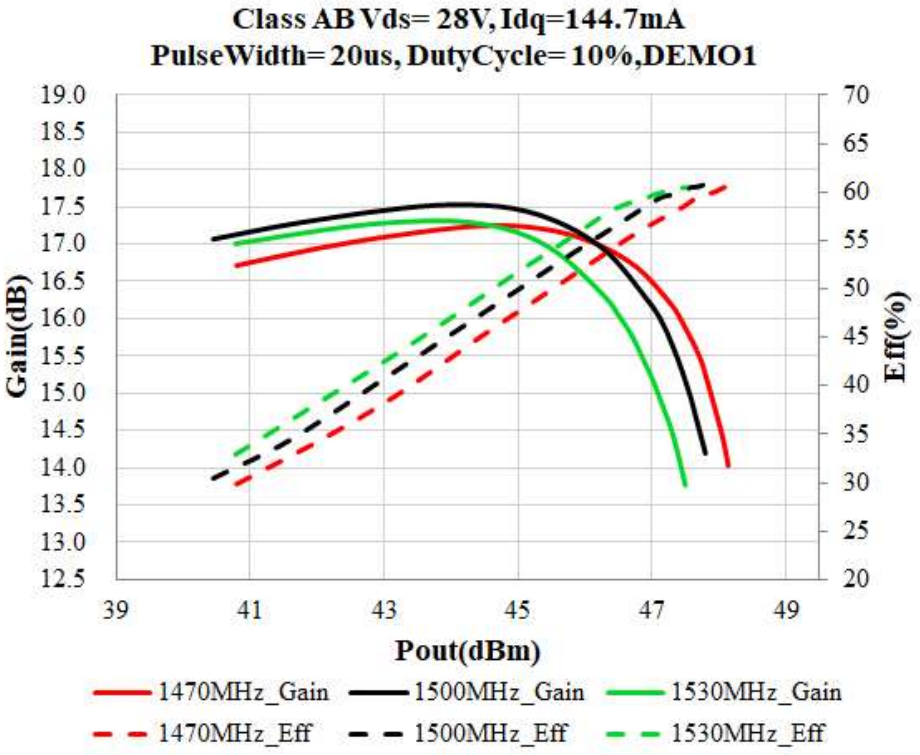
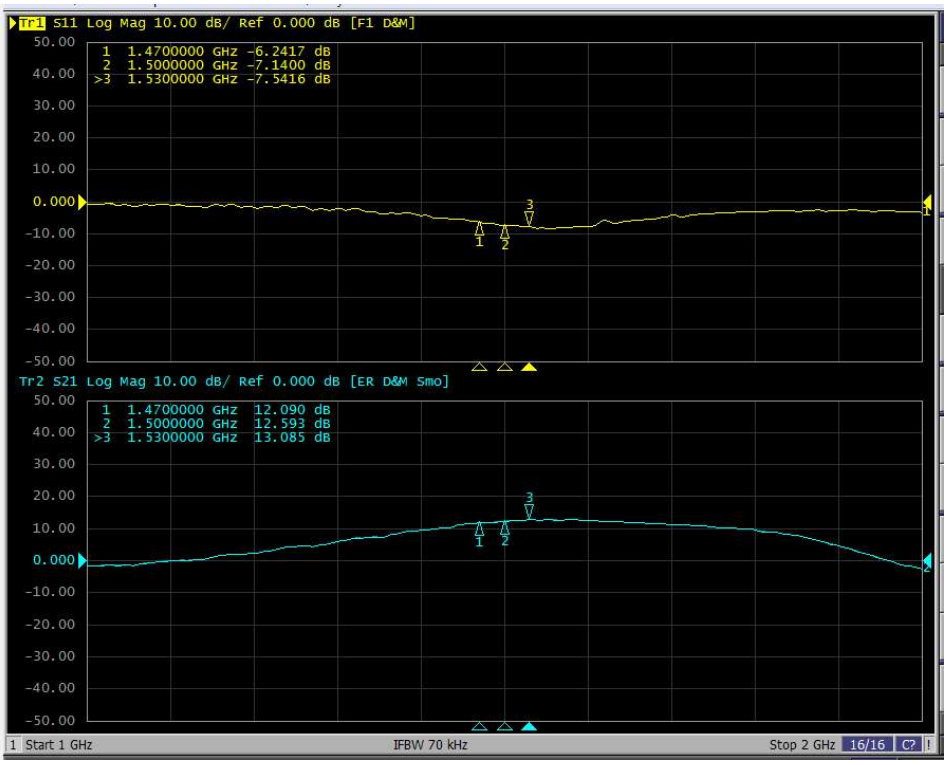


Figure 4.Network analyzer output S11/S21



1.3GHz application board

Reference Circuit of Test Fixture Assembly Diagram
20mils RO4350B

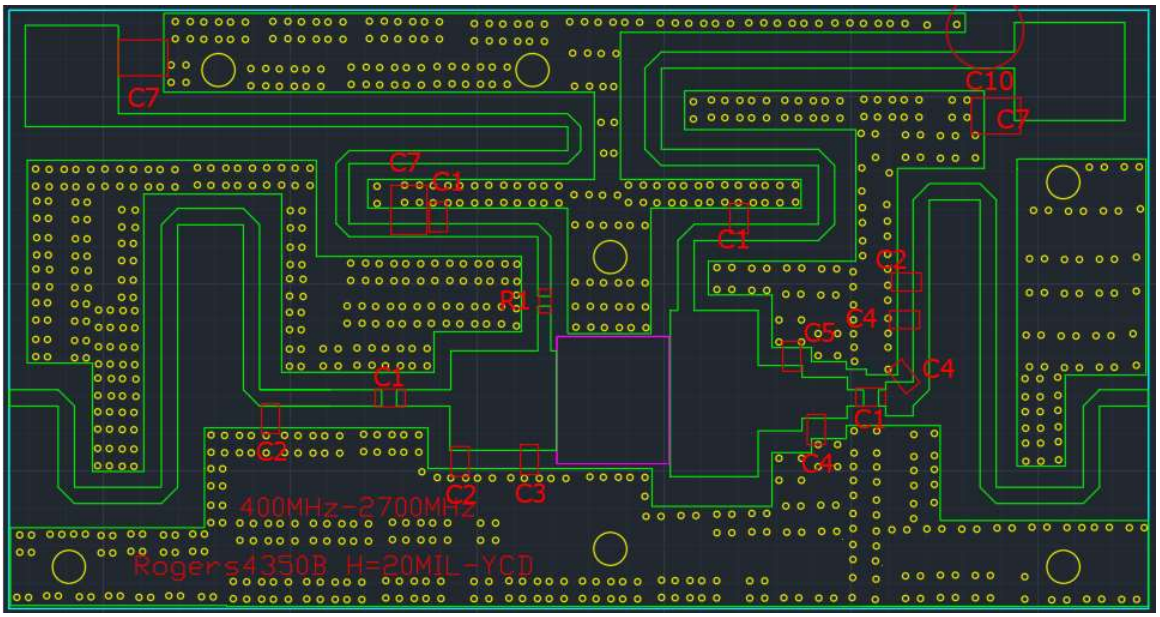


Figure 6. Test Circuit Component Layout

Table 6. Test Circuit Component Designations and Values

Component	Value	Quantity
U1	ITDE15050E2	1
C1	30pF	4
C7	10uF/63V	3
R1	10Ω	1
C10	470uF/63V	1
C3	6.8pF	1
C2	2pF	3
C5	8.2pF	1
C4	1pF	3

TYPICAL CHARACTERISTICS

Figure 7. Power Gain and Drain Efficiency as function of Power Output at Idq =20mA

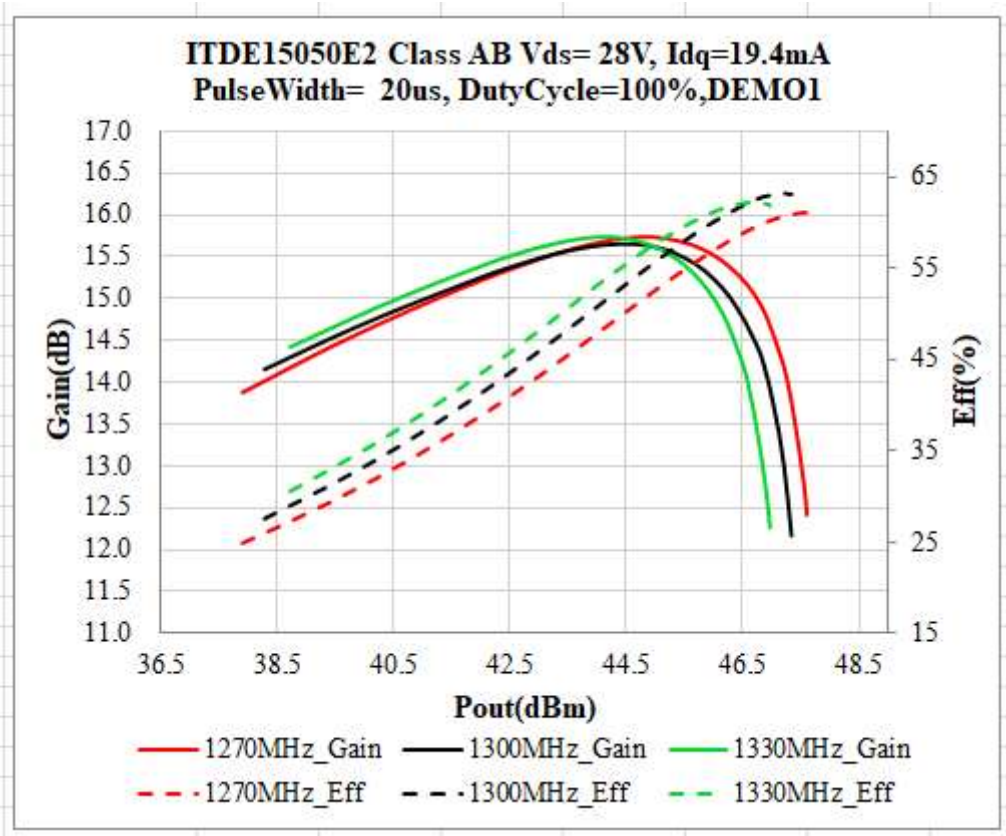
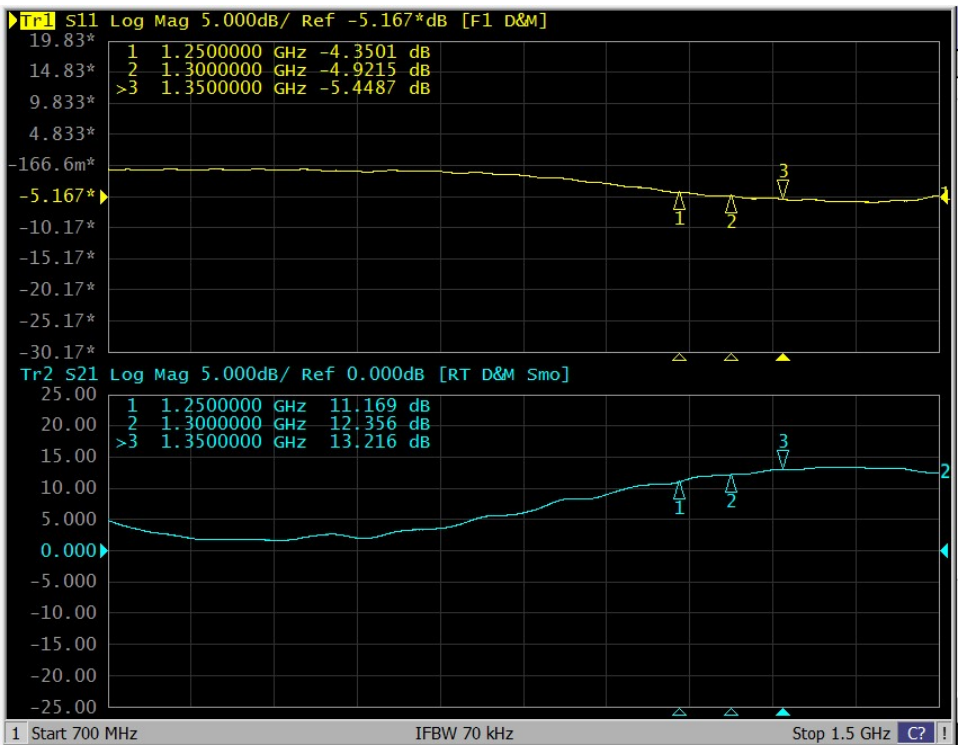


Figure 8.Network analyzer output S11/S21



900MHz application board

Reference Circuit of Test Fixture Assembly Diagram
20mils RO4350B

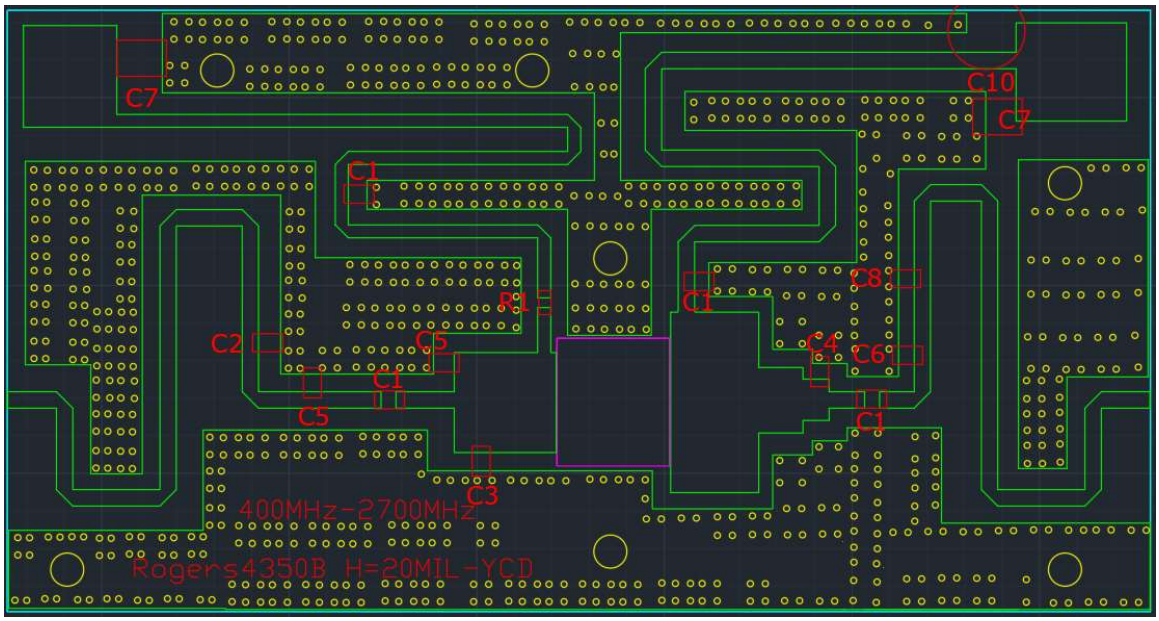


Figure 10. Test Circuit Component Layout

Table 7. Test Circuit Component Designations and Values

Component	Value	Quantity
U1	ITDE15050E2	1
C1	47pF	4
C7	10uF/63V	2
R1	10Ω	1
C10	470uF/63V	1
C3	15pF	1
C2	3pF	1
C5	3.9pF	2
C4	8.2pF	1
C6	4.7pF	1
C8	2.7pF	1

TYPICAL CHARACTERISTICS

Figure 11. Power Gain and Drain Efficiency as function of Power Output at Idq =20mA

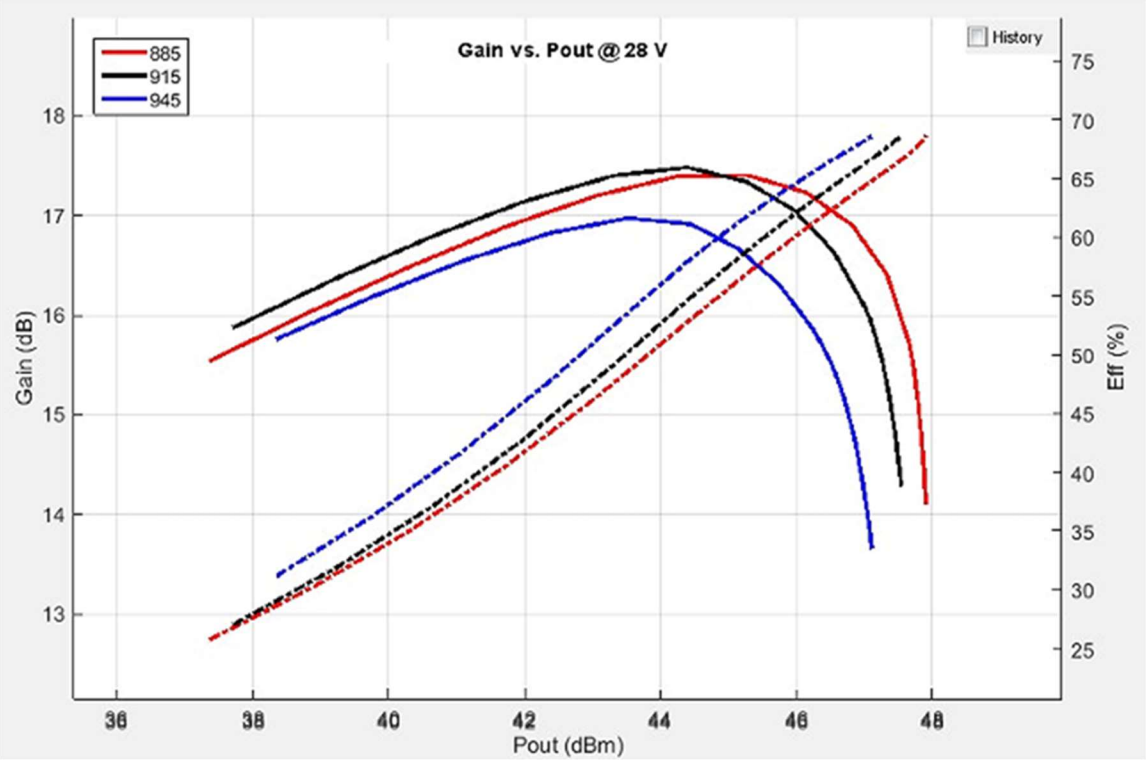
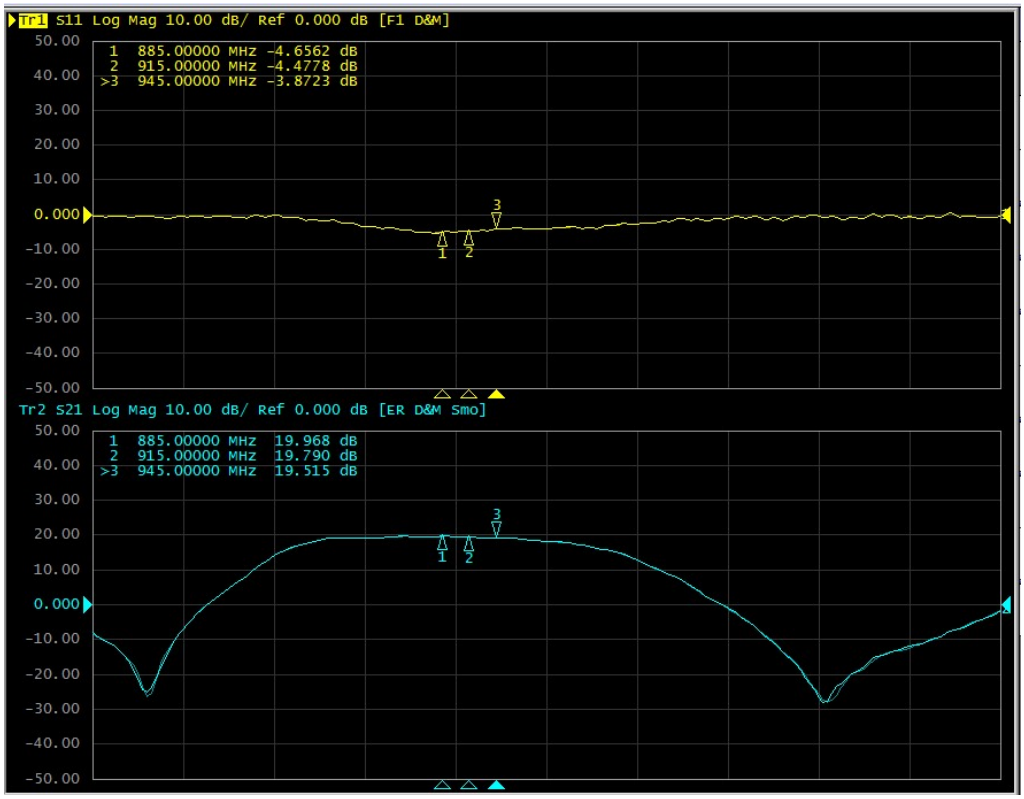
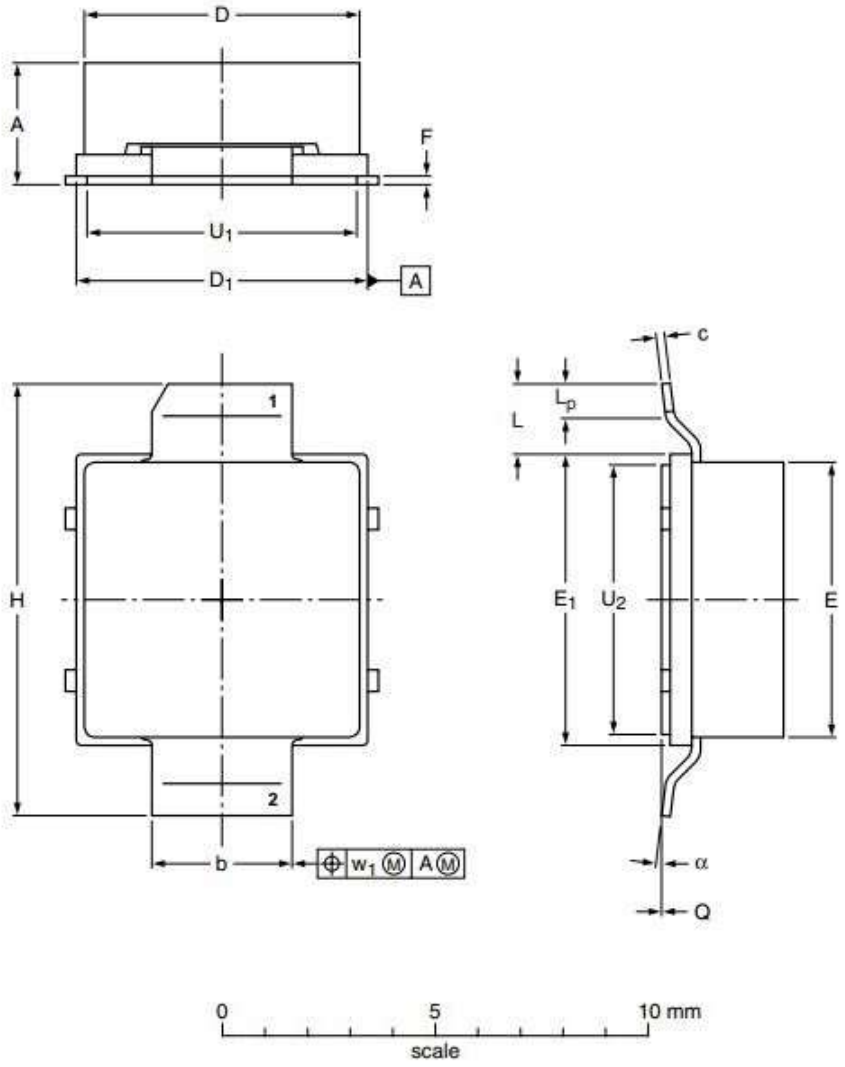


Figure 12.Network analyzer output S11/S21



Package Outline

Earless Flanged ceramic package; 2 leads（1-Drain、2-Gate、Flange-GND）



UNIT	A	b	c	D	D_1	E	E_1	F	H	L	L_P	Q	U_1	U_2	w_1	α
mm	3.63 3.05	3.38 3.23	0.23 0.18	6.55 6.40	6.93 6.78	6.55 6.40	6.93 6.78	0.23 0.18	10.29 10.03	1.65	1.02 0.51	+0.05 −0.05	6.43 6.27	6.43 6.27	0.51	7° 0°
inches	0.143 0.120	0.133 0.127	0.009 0.007	0.258 0.252	0.273 0.267	0.258 0.252	0.273 0.267	0.009 0.007	0.405 0.395	0.065	0.040 0.020	+0.002 −0.002	0.253 0.247	0.253 0.247	0.02	7° 0°

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-E2A					03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2023/8/31	Rev 1.0	Product Datasheet
2023/9/5	Rev 1.1	Add 1.3G, 900MHz data

Application data based on ZXY-23-09/10/11

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