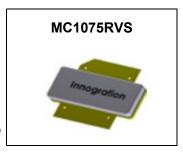
700W,50V High Power RF LDMOS FETs

Description

The MC1075RVS itself is a 700-watt capable, high performance, unmatched single ended LDMOS FET.

It is recommended to use paired MC1075RVS to enable 1400W designed for ISM application with frequencies HF to 500MHz. Compared to similar power level but in single dual-path packaged device, it offers better thermal management and easier maintenance.

Demonstration of paired MC1075RVS(right) Vs single dual-path device(left) at 250MHz





Typical performance(on 162.5MHz narrow band application board with 2×MC1075RVS devices soldered)

V_{DS}=50V,I_{DQ}=400mA, CW,

Freq(MHz)	P _{out} (W)	Pin(dBm)	Gain(dB)	η(%)
162.5	1400	41	20.5	74

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift

Suitable Applications

- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 160-230MHz (TV VHF III)
- 136-174MHz (Commercial ground communication)

- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- · Pb-free, RoHS-compliant
- Laser Exciter
- Synchrotron
- MRI
- Plasma generator
- Weather Radar

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
DrainSource Voltage	V _{DSS}	+115	Vdc
GateSource Voltage	V _{GS}	-10 to +10	Vdc
Operating Voltage	V _{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	Tc	+150	°C
Operating Junction Temperature	T _J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case			
T _C = 85°C, 1400W Pulsed CW output,162.5MHz, 2 pcs of MC1075RVS	Rejc	0.1	°C/W
combined, CW			

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22A114)	Class 2

Table 4. Electrical Characteristics (T_A = 25 ℃ unless otherwise noted)

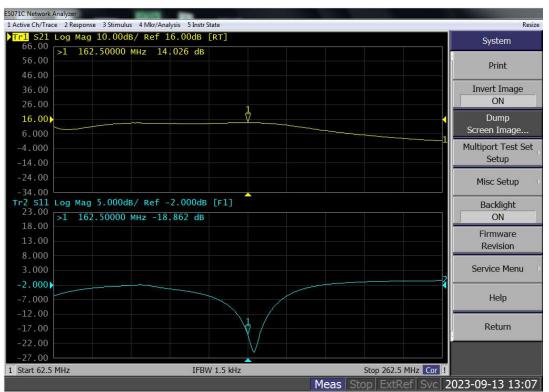
Characteristic	Symbol	Min	Тур	Max	Unit
DC Characteristics (per half section)					
Drain-Source Voltage	\ \/		115		V
V _{GS} =0, I _{DS} =1.0mA	V _{(BR)DSS}		115		
Zero Gate Voltage Drain Leakage Current				1	
$(V_{DS} = 75V, V_{GS} = 0 V)$	I _{DSS}			I	μΑ
Zero Gate Voltage Drain Leakage Current				1	
$(V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V})$	I _{DSS}	1	μΑ		
GateSource Leakage Current				1	μА
$(V_{GS} = 10 \text{ V}, V_{DS} = 0 \text{ V})$	I _{GSS}				
Gate Threshold Voltage	V _{GS} (th)		2.0		V
$(V_{DS} = 50V, I_D = 600 \mu A)$	V GS(U1)		2.0		V
Gate Quiescent Voltage	$V_{GS(Q)}$		3.2		V
$(V_{DD} = 50 \text{ V}, I_D = 400 \text{ mA}, \text{Measured in Functional Test})$	V GS(Q)		5.2		V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): $V_{DD} = 50 \text{ Vdc}$, $I_{DQ} = 200 \text{ mA}$, f = 162.5 MHz, pulse width:100us, duty cycle:10%, 2 piece of MC1075RVS combined

Open and short, at 1400W Pulsed CW Output Power	No Device Degradation
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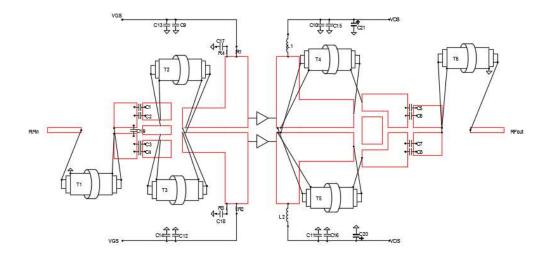
TYPICAL CHARACTERISTICS

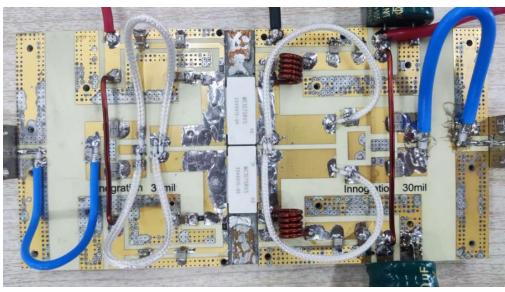
Figure 1: Network analyzer output S11/S21 Vds=50V, Idq=400mA, Pin=0dBm



MC1075RVS LDMOS TRANSISTOR

Reference Circuit of Test Fixture (162.5MHz Pulsed CW Power Amplifier)

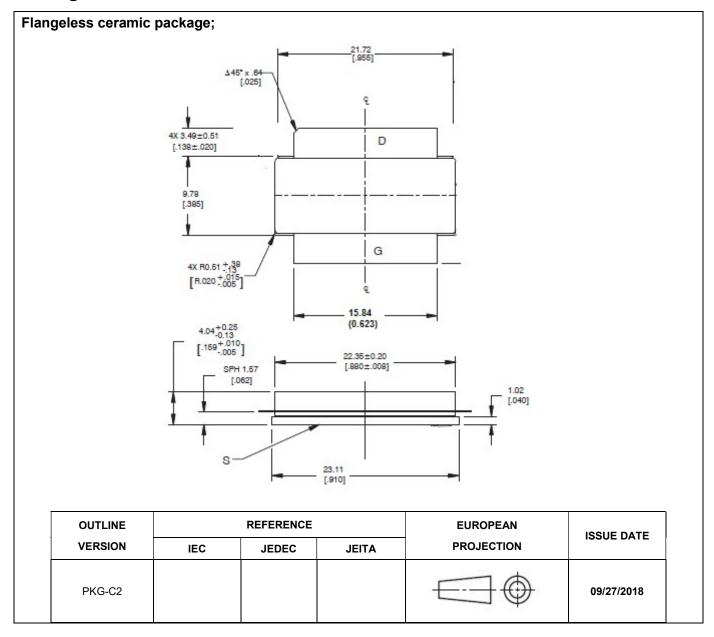




Component	Description	Suggestion	
C1~C12	C1~C12 470pF		
C14~C18	10uF	10uF/100V	
C19	47pF	MQ301111	
C20,C21	4700uF/63V		
R1~R4	18 Ω	1206	
L1,L2	5 Turns, d=5mm D=1.5mm	4700uF/63V	
T1	50ohm 10mm	SF-086-50	
T2,T3	12.5ohm 10mm	SFF-12.5-1.5	
T4,T5	16.7ohm 10mm	SFF-16.7-1.5	
T6	35ohm	SFF-25-3	
T4,T5	12.5ohm 10mm	SFF-12.5-3	
T6	16.7ohm	SFF-16.7-1.5	

MC1075RVS LDMOS TRANSISTOR

Package Outline



MC1075RVS LDMOS TRANSISTOR

Document Number: MC1075RVS Preliminary Datasheet V1.0

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2023/9/13	Rev 1.0	Preliminary datasheet

Application data based on HL-23-42

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