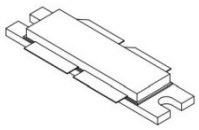
MQ011K2VPX LDMOS TRANSISTOR

Document Number: MQ011K2VPX
Preliminary Datasheet V1.8

1200W, 50V High Power RF LDMOS FETs

MQ011K2VPX



Description

The MQ011K2VPX is a 1200W capable, highly rugged, unmatched LDMOS FET, designed for commercial and industrial applications with frequencies HF to 300MHz.

It is featured for industry leading high power and high ruggedness, suitable for Industrial, Scientific and Medical application, as well as HF communication, VHF TV and Aerospace applications.

- FM band: 88-108MHz CW application data

Trade off	Voltage(V)	Idq（mA）	Pin(dBm)	Pout(W)	Power Gain(dB)	Eff(%)
High Power	50	200	39.5	>1250	22.5	>75
High Efficiency	50	200	38	>1000	22	>80

Features

- High breakdown voltage enable class E operation
- High Efficiency and Linear Gain Operations
- On chip RC network enable high stability and ruggedness
- Integrated ESD Protection
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain—Source Voltage	V_{DSS}	140	Vdc
Gate—Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case ,Case Temperature 85°C, 1100W CW, 50 Vdc, I_{DQ} = 200 mA	$R_{\theta JC}$	0.1	°C/W
Transient thermal impedance from junction to case Tj = 150° C; tp = 100 us; Duty cycle = 20 %	Zth	0.015	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22—A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0V, I_{DS}=1.0mA	$V_{(BR)DSS}$		140		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate—Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS(th)}$	——	2.5	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 200 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.2	——	V
Drain source on state resistance (V_{DS} = 0.1V, V_{GS} = 10 V) Each section side of device measured	Rds(on)		54		mΩ
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{ISS}		400		Pf
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{OSS}		120		Pf
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{RSS}		2		Pf

TYPICAL CHARACTERISTICS (108MHz)

Higher power tuning

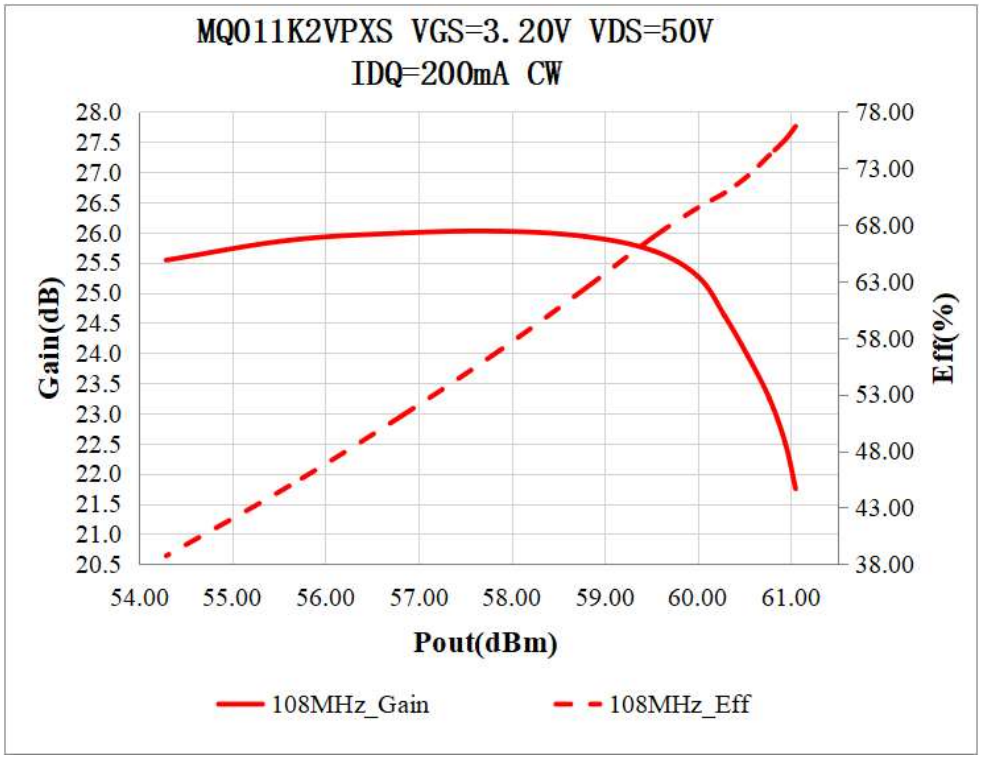


Figure 1: Efficiency and power gain as the function of Pout (Vds=50V, Idq=200mA,CW)

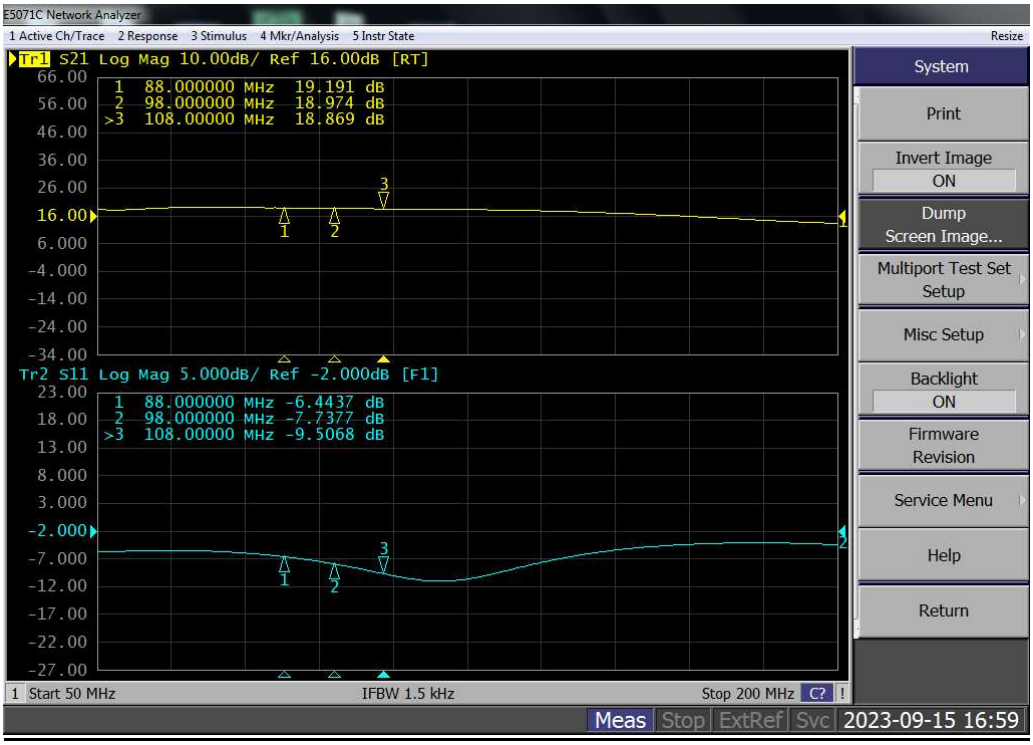
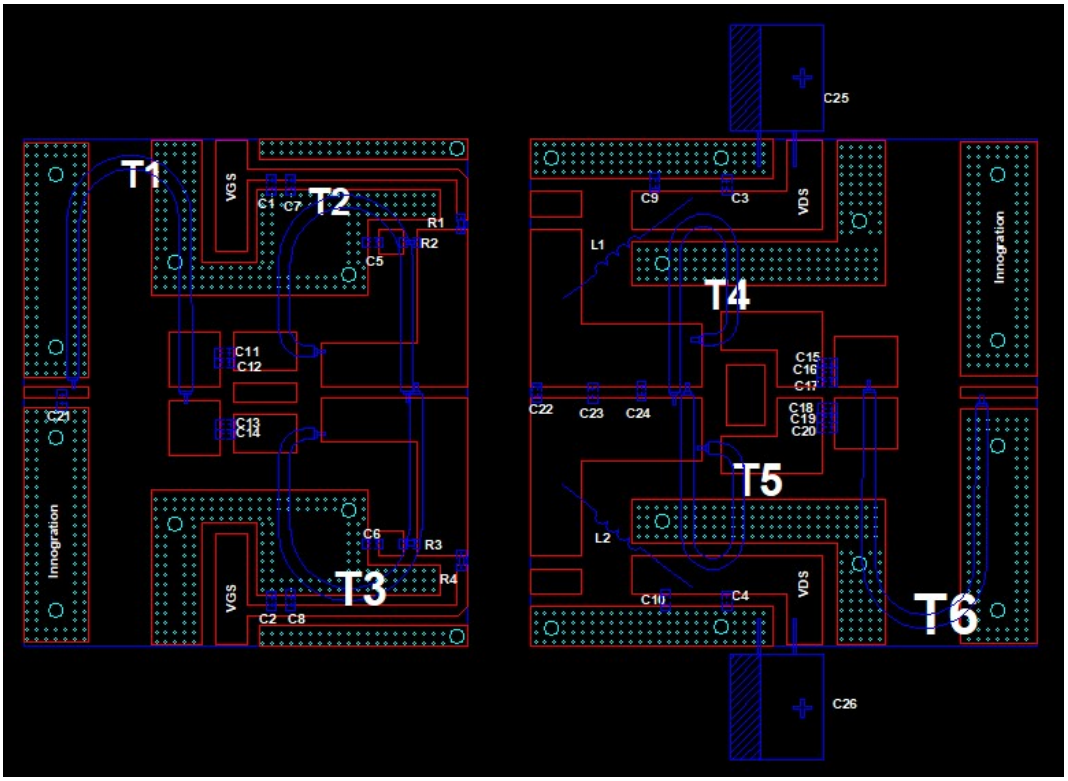


Figure 2: Network analyzer output, S11/S21 (Vds=50V,Idq=500mA, Vgs=3.3V)



Component	Description	Suggestion
C7~C10	10nF/100V	Ceramic multilayer capacitor
C1~C6	10uF/100V	Ceramic multilayer capacitor
C11~C20	560pF	MQ101111
C21	12pF	MQ101111
C22	22pF	MQ101111
C23	15pF	MQ101111
C24	27pF	MQ101111
C25,C26	4700uF/63V	Electrolytic Capacitor
R1，R2	18Ω	Chip Resistor
R3，R4	51Ω	Chip Resistor
T1	50ohm,200mm	RFSFBU-086-50
T2,T3	12.5 ohm ,200mm	SFF-12.5-1.5
T4,T5	16.7ohm，200mm	SFF-16.7-1.5
T6	35 ohm，250mm	SFF-35-3
L1,L2	1.5mm ，8 turns D=5mm	DIY air core inductance

TYPICAL CHARACTERISTICS (108MHz)

Higher Efficiency tuning

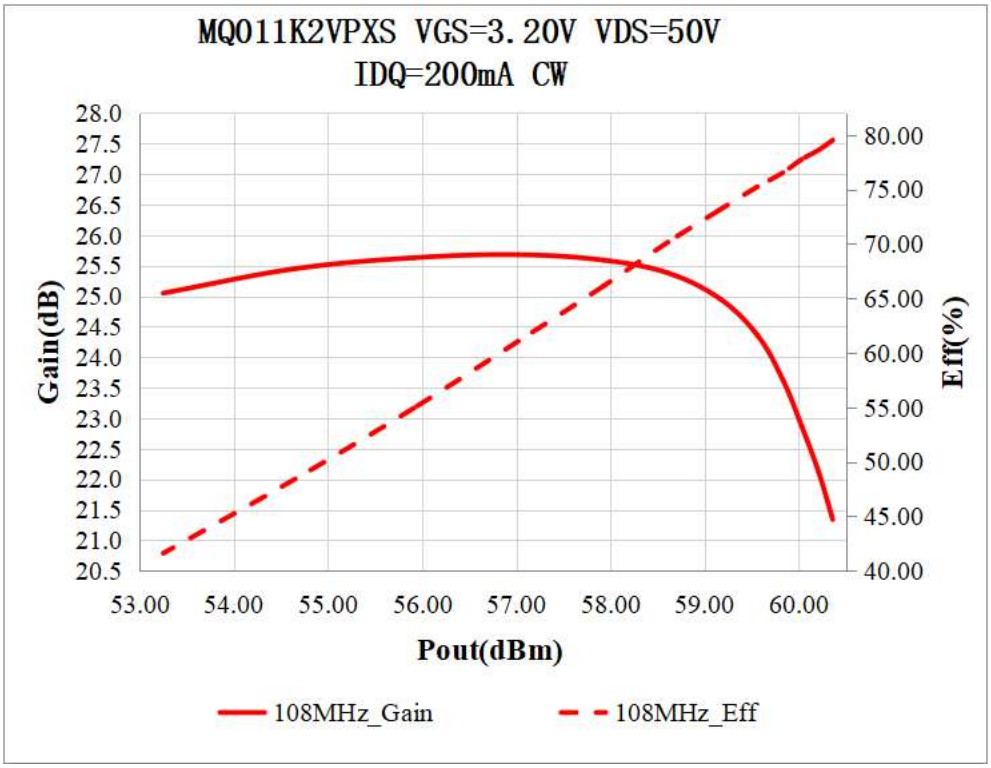


Figure 3: Efficiency and power gain as the function of Pout (Vds=50V, Idq=200mA,CW)

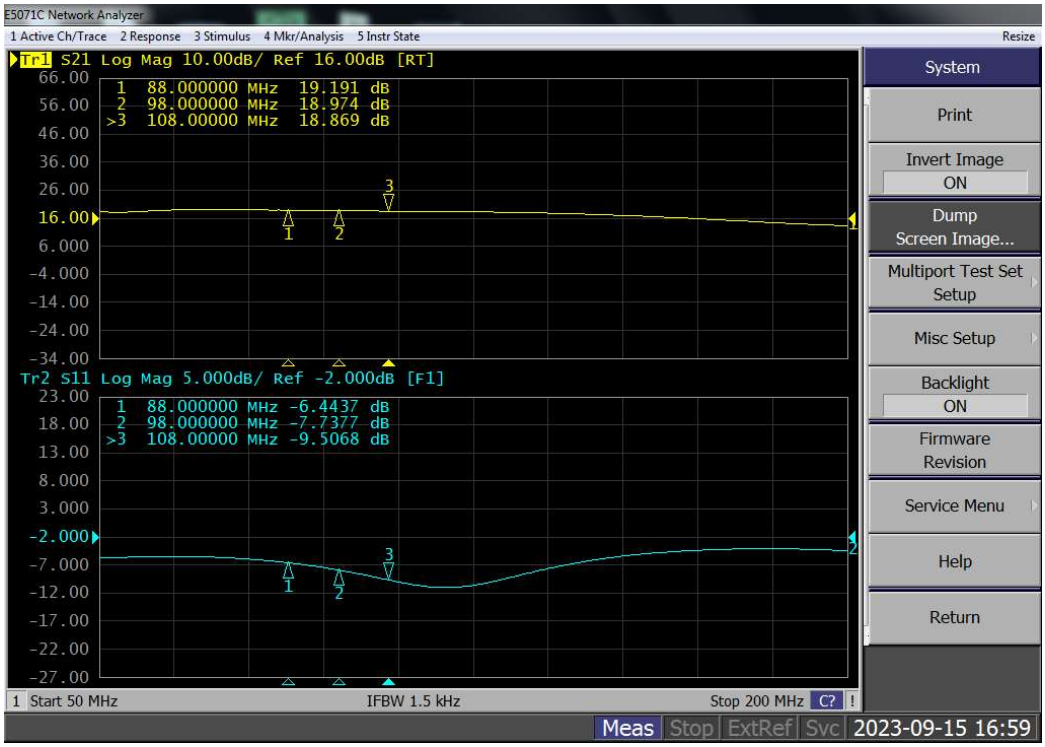
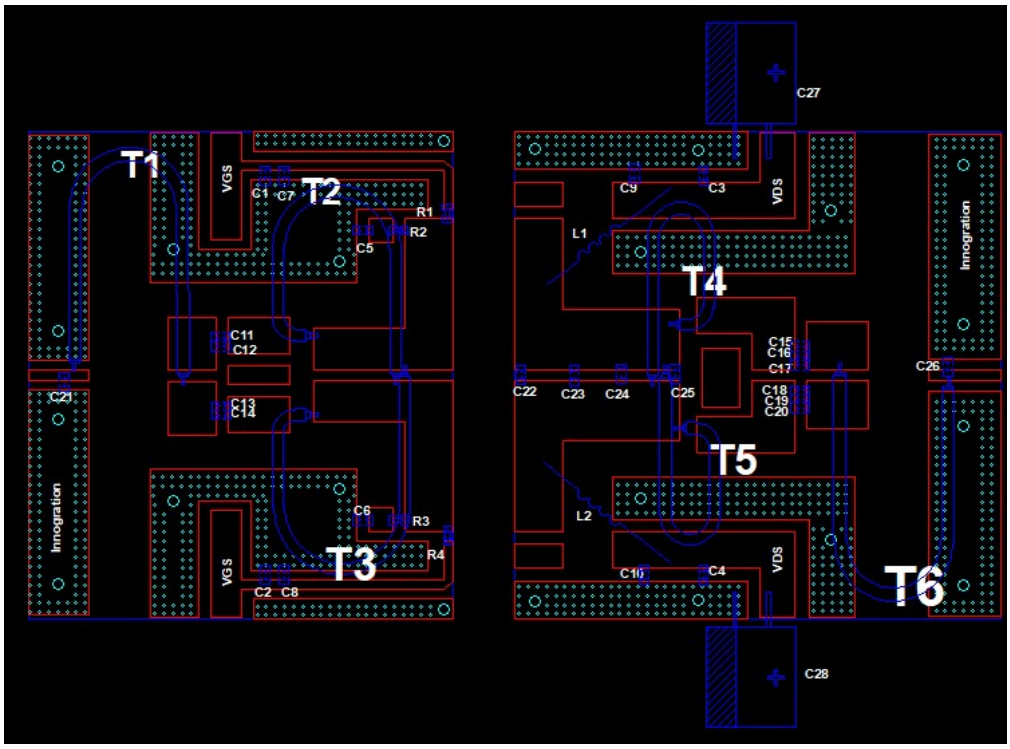


Figure 4: Network analyzer output, S11/S21 (Vds=50V,Idq=500mA, Vgs=3.3V)



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C1~C6	10uF/100V	Ceramic multilayer capacitor
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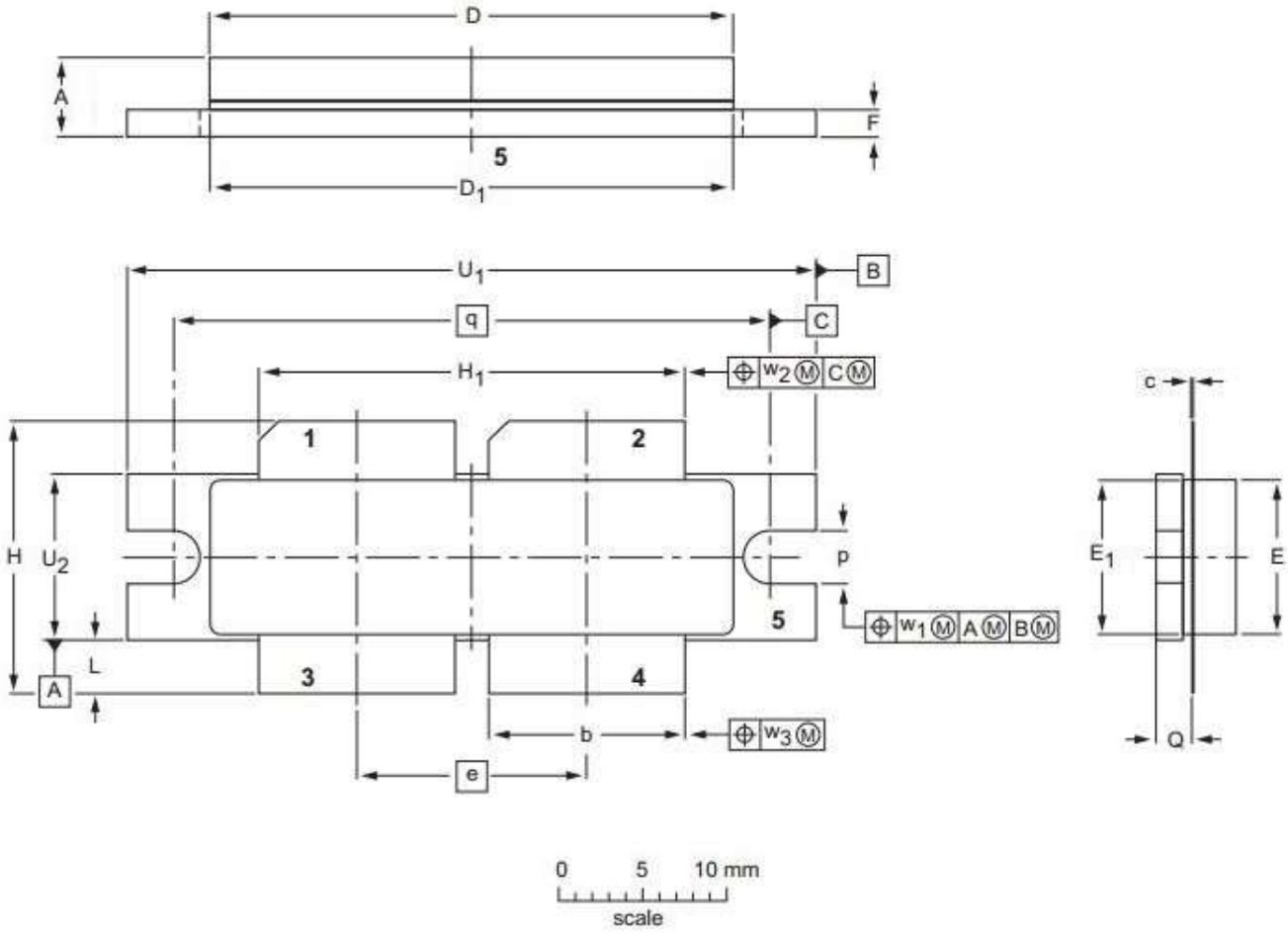
C23	15pF	MQ101111
C24	27pF	MQ101111
C25	10pF	MQ101111
C26	5.1pF	MQ101111
C27,C28	4700uF/63V	Electrolytic Capacitor
R1，R2	18Ω	Chip Resistor
R3，R4	51Ω	Chip Resistor
T1	50ohm,200mm	RFSFBU-086-50
T2,T3	12.5 ohm ,200mm	SFF-12.5-1.5
T4,T5	16.7ohm，200mm	SFF-16.7-1.5
T6	50 ohm，200mm	SFF-50-3
L1,L2	1.5mm,8 turns,D=5mm	DIY air core inductance

Package Outline

Flanged ceramic package; 2 mounting holes; 4 leads（1、2—DRAIN、3、4—GATE、5—SOURCE）



UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	W_1	W_2	W_2
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	3.30 3.05	2.26 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.130 0.120	0.089 0.079	1.400	1.625 1.615	0.405 0.395	0.01	0.02	0.01

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4E					03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2023/9/15	Rev 1.0	Preliminary Datasheet

Application data based on TC-23-59

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