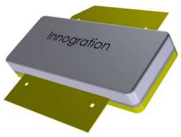
915MHz, 450W, 40V High Power RF LDMOS FETs

ITDE10450C2



Description

The ITDE10450C2 is a 450-watt, internally matched LDMOS FET, designed for ISM applications including RF Energy at 915MHz. It Can be used in Class AB/B and Class C configuration, supporting both CW and pulsed signal

In typical application using 2*ITDE10450C2 in parallel, it can deliver more than 850W CW with high efficiency

- Typical Performance using single **ITDE10450C2** (On Innogration fixture with device soldered):

VDD = 40 Volts, I_{DQ} = 50 mA, CW signal

Freq(MHz)	Pin(dBm)	Pout(dBm)	Pout(W)	IDS(A)	Gain(dB)	EFF(%)
915	40	56.7	470	16.7	16.7	70.0%

- Typical Performance using **ITDE10450C2*2** (On Innogration fixture with device soldered):

VDD = 40 Volts, I_{DQ} = 50 mA, CW signal

Freq(MHz)	Pin(dBm)	Pout(dBm)	Pout(W)	IDS(A)	Gain(dB)	EFF(%)
915	43	59.5	880	34.5	16.5	64.0%

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	95	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+42	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	0.15	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit

DC Characteristics (per half section)

Drain-Source Breakdown Voltage (V_{GS}=0V; I_D=100uA)	V_{DSS}	95	——	——	V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 40 V, V_{GS} = 0 V)	I_{DSS}	——	——	10	μA
Gate--Source Leakage Current (V_{GS} = 6 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 40V, I_D = 600 uA)	$V_{GS(th)}$	——	2.0	——	V
Gate Quiescent Voltage (V_{DD} = 40 V, I_{DQ} = 100 mA, Measured in Functional Test)	$V_{GS(Q)}$	2.1	2.62	3.1	V

Functional Tests (On Innogration Test Fixture, 50 ohm system) :V_{DD} =40 Vdc, I_{DQ} = 50 mA, f = 915 MHz, Pin=43dBm CW Signal Measurements.

Power Gain	G_p	——	16.5	——	dB
Drain Efficiency @ P_{OUT}	η_D	——	64	——	%
Output Power	P_{out}	——	850	——	W
Input Return Loss	IRL	——	-7	——	dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 40 Vdc, I_{DQ} = 50 mA, f = 915 MHz

VSWR 10:1 at 850W Output Power at all Phase Angles, pulsed CW, 100us, 10%	No Device Degradation

Reference Circuit of Test Fixture Assembly Diagram 1*ITDE10450C2

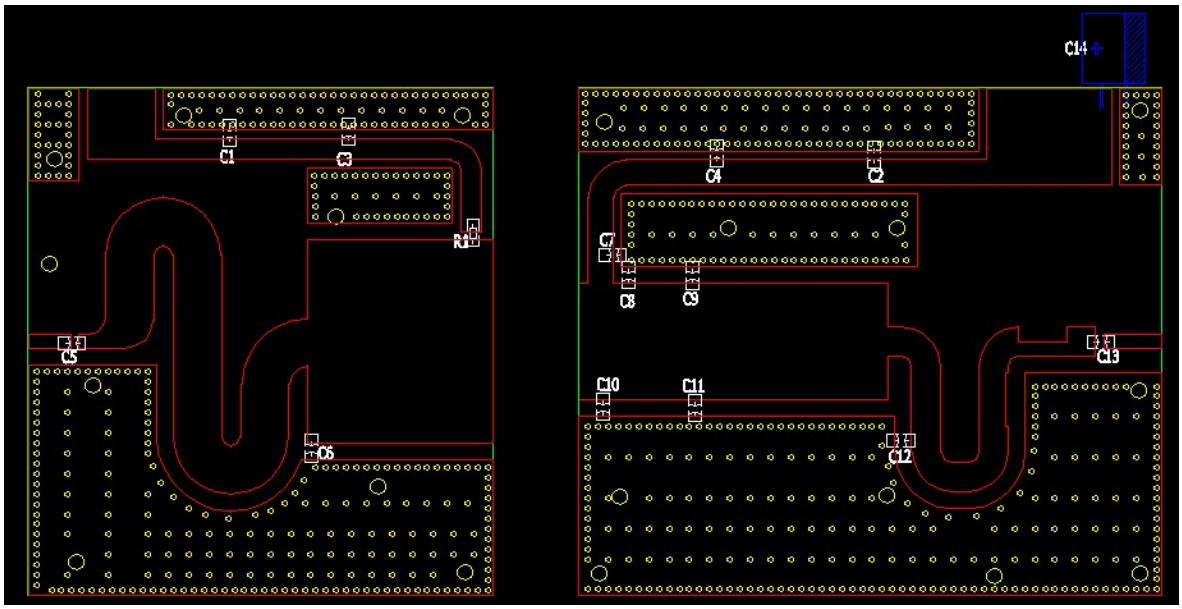


Figure 1. Test Circuit Component Layout

Table 1. Test Circuit Component Designations and Values

Component	Description	Suggestion
C1,C2	10uF	10uF/100V
C3,C4,C5	56pF	MQ101111
C6	7.5pF	MQ101111
C14	2000uF/63V	Electrolyic Capacitor
R1	10 Ω	Chip Resistor
C7	9.1pF	MQ101111
C8	12pF	MQ101111
C9	8.2pF	MQ101111
C10	11pF	MQ101111
C11	10pF	MQ101111
C12	0.5pF	MQ101111
C13	47pF	MCM-1-300V-D-470J
PCB	30mil Rogers 4350B	

TYPICAL CHARACTERISTICS

Figure 2. Drain Efficiency and Power Gain as Function of CW Output Power

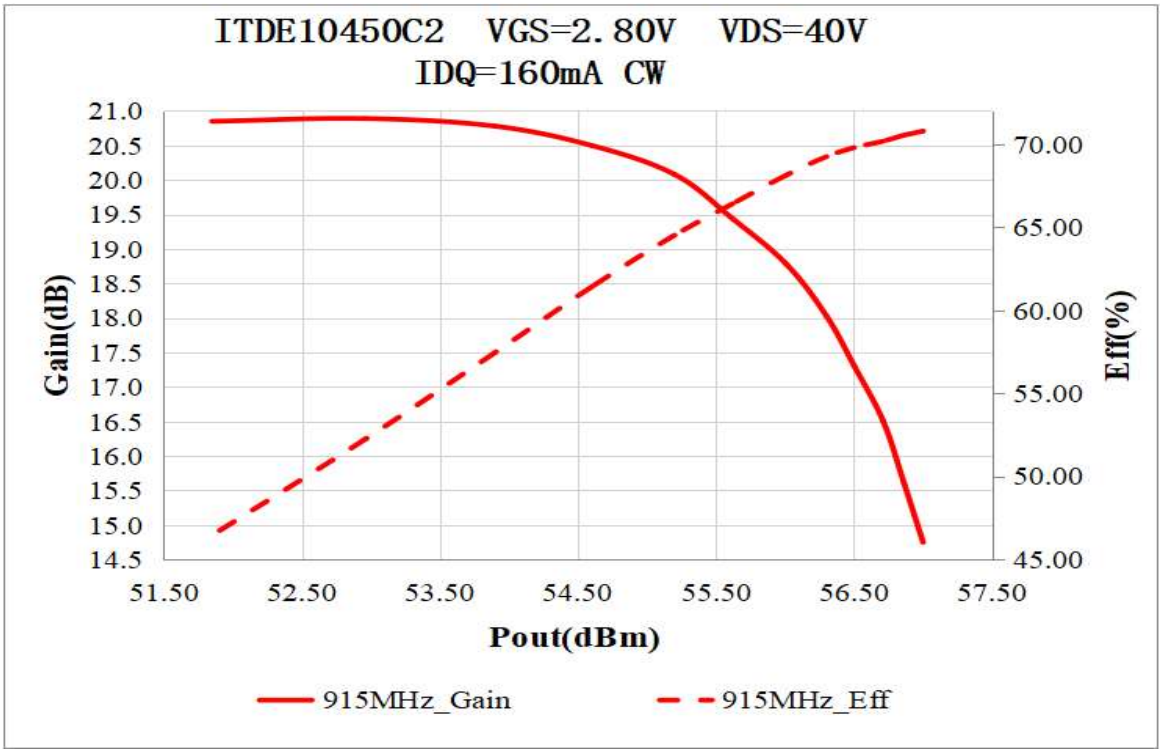
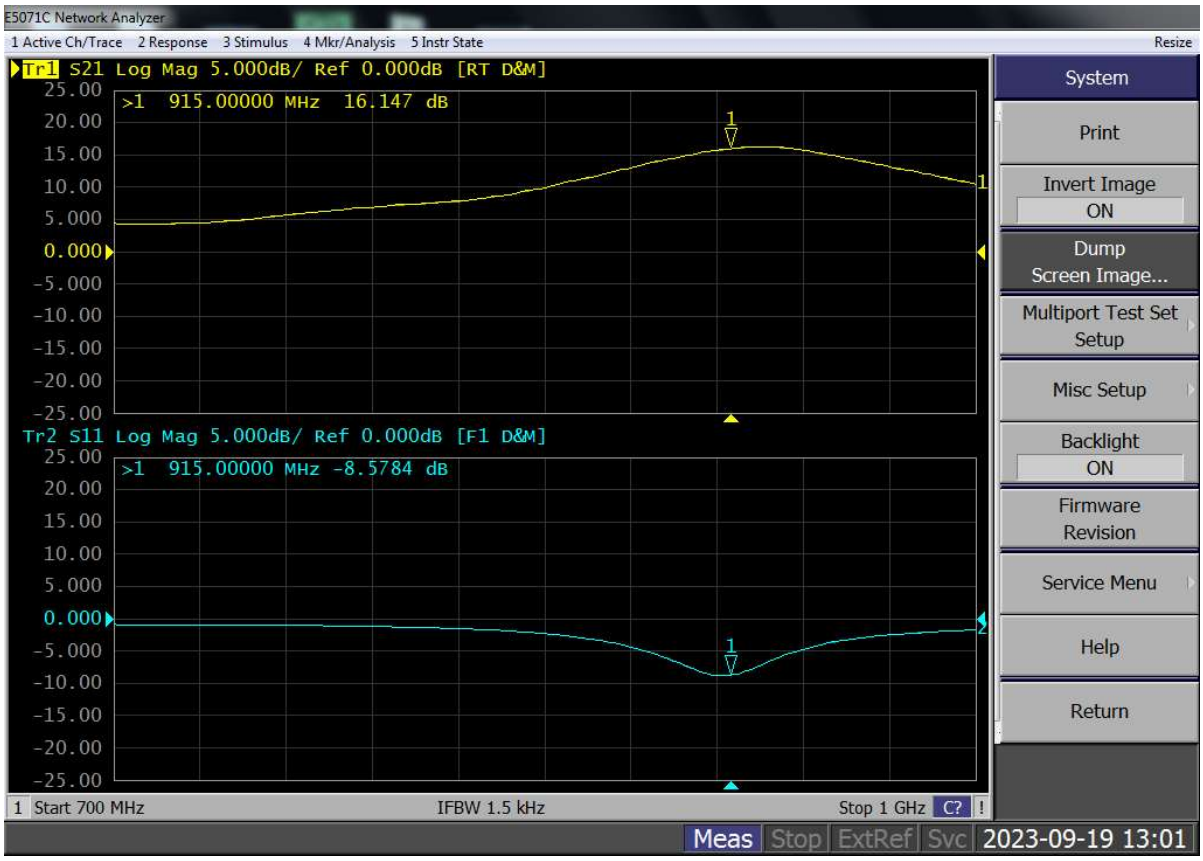


Figure 3. Network analyzer output S11/S21



Reference Circuit of Test Fixture Assembly Diagram
2*ITDE10450C2

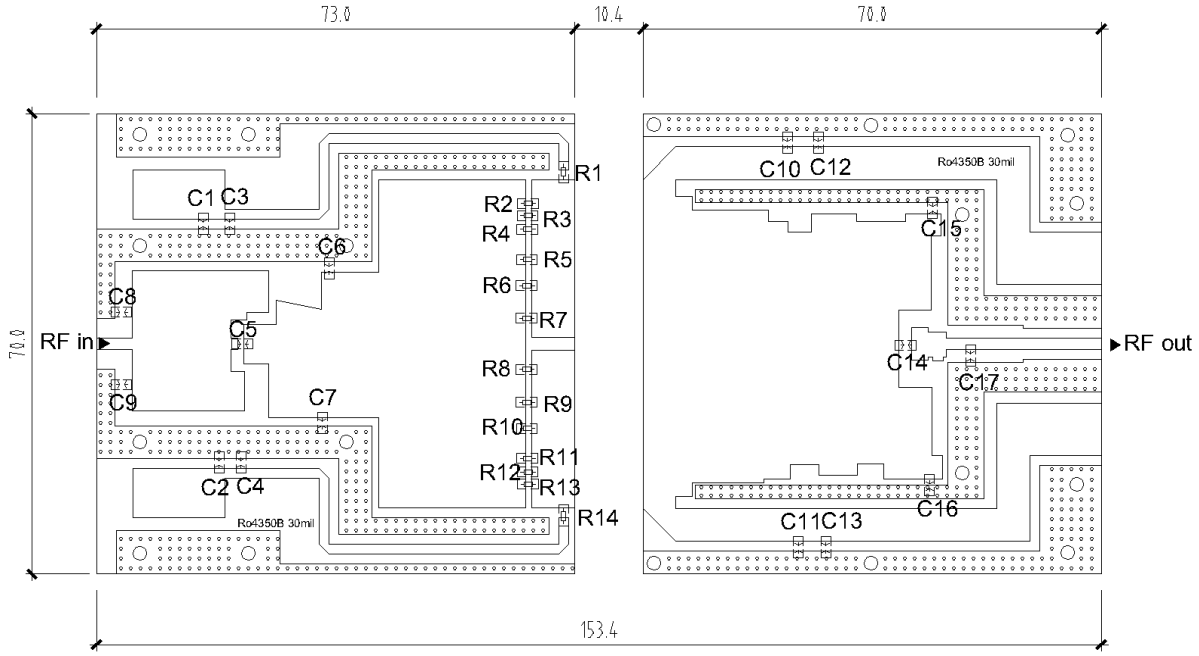


Figure 3. Test Circuit Component Layout

Table 2. Test Circuit Component Designations and Values

Component	Description	Suggested Types
C1、C2、C5、C10、C11	56pF	ATC800B
C14	56pF*3	ATC800B
C3、C4、C12、C13	Ceramic multilayer capacitor, 10uF	
C6	3.3pF	ATC800B
C7	5.6pF	ATC800B
C8	3.3pF	ATC800B
C9	1pF	ATC800B
C15、C16、C17	0.5pF	ATC800B
R1~R14	Chip Resistor,9.1Ω,1206	
PCB	30mil thickness,RO4350B	

TYPICAL CHARACTERISTICS

Figure 4. Drain Efficiency and Power Gain as Function of CW Output Power

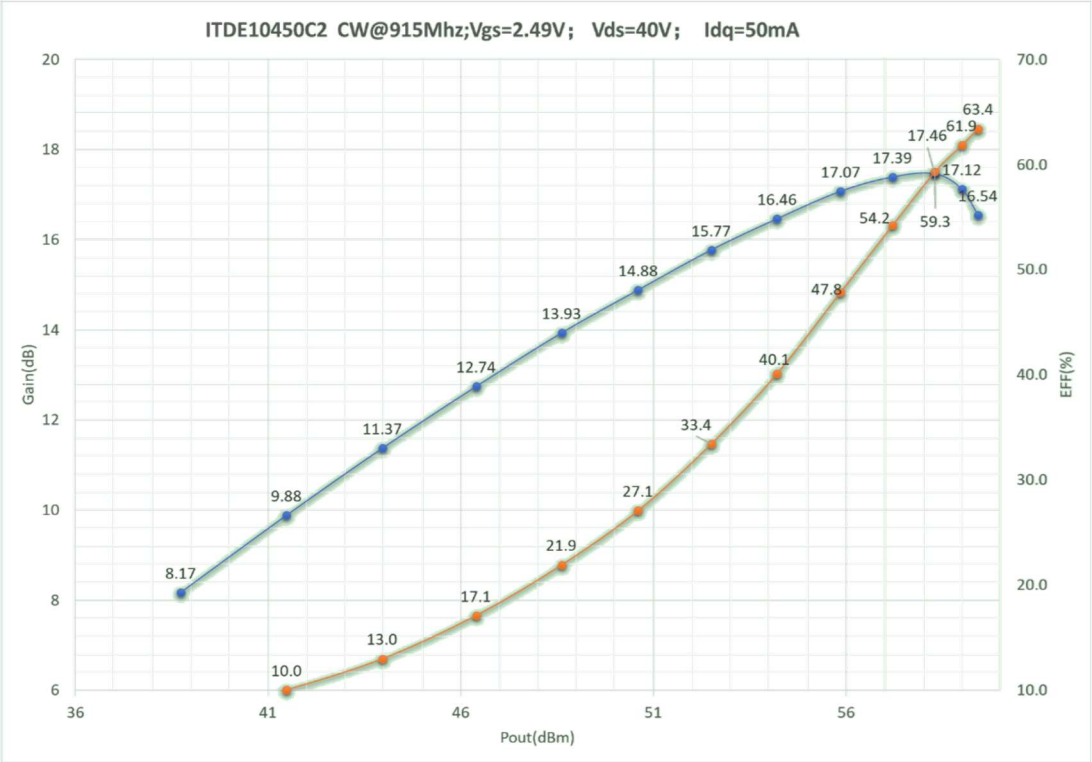
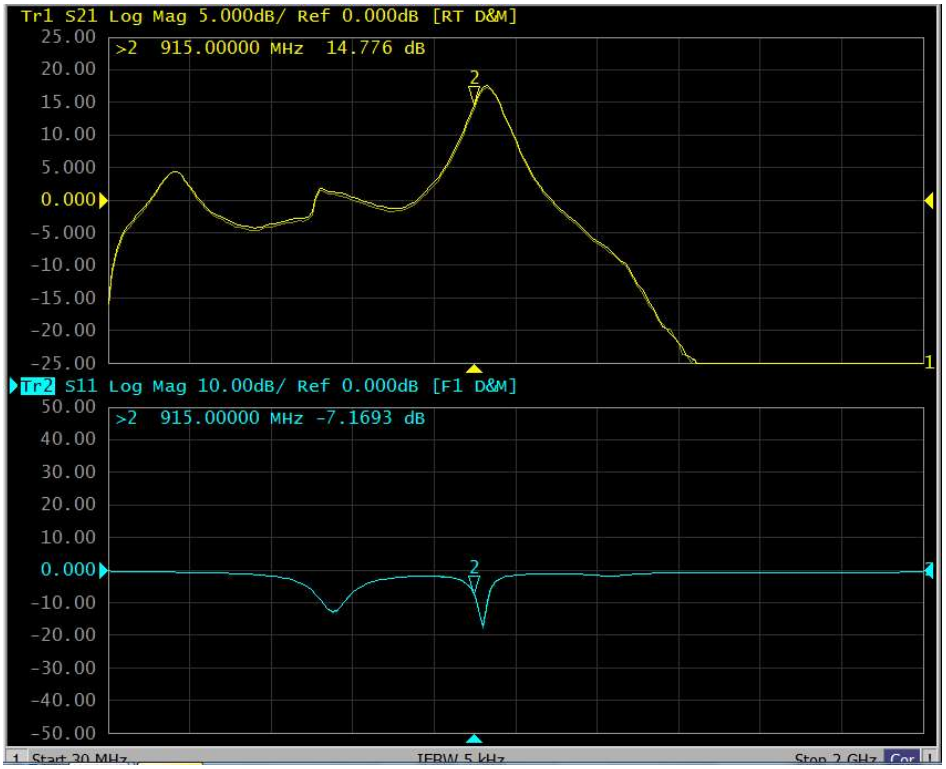
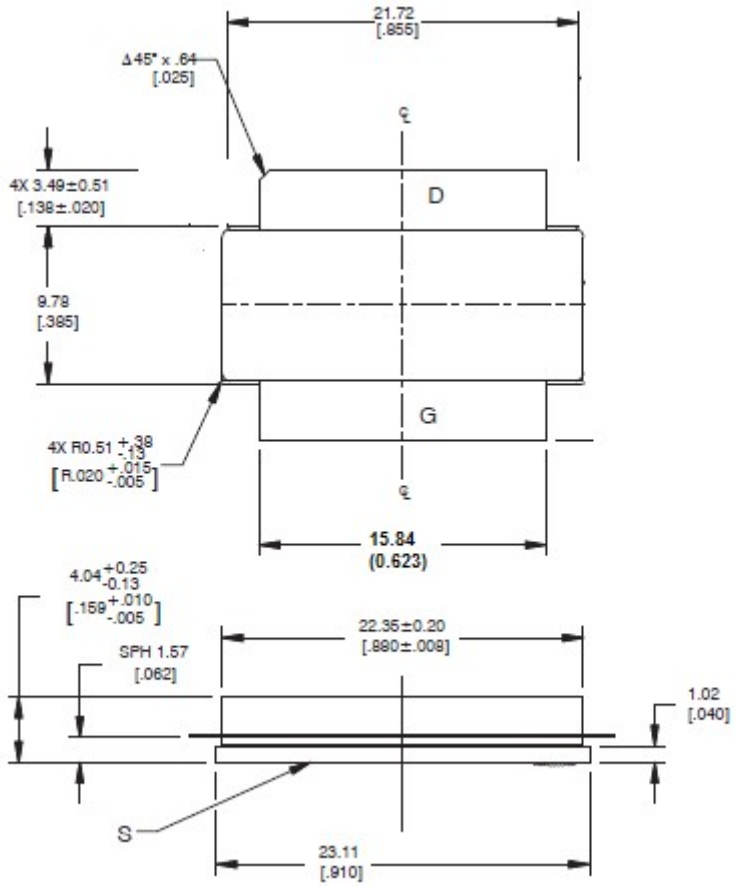


Figure 3. Network analyzer output S11/S21



Package Outline

Flangeless ceramic package;



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-C2					09/27/2018

Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2022/1/12	Rev 1.0	Preliminary Datasheet
2023/9/19	Rev 1.1	Add single device application data

Application data based on JF-21-14/TC-23-60

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