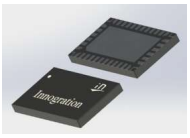
50W,50V Plastic RF LDMOS Transistor

ITGV10051C6



Description

The ITGV10051C6 is a dual path 50-watt, highly rugged, LDMOS transistor, designed for any general applications at frequencies up to 1GHz, in 10*6mm QFN plastic package, supporting surface mounted on PCB through high density grounding vias.

It can be configured as Doherty to be as high efficiency and low cost driver for 4G/5G application within 0.6-1GHz.

- Typical Doherty RF Performance (On Innogration fixture with device soldered).

Vds=50V Idq_main=55mA, Vgs_peak=2.4V

Freq (MHz)	Pulse CW Signal			P_{avg}=37dBm WCDMA Signal		
	Gain P1dB (dB)	P3dB (W)	Eff@P3dB (%)	Gp (dB)	Eff(%)	$ACPR_{5M}$ (dBc)
758	14.9	52	66	15.2	42.5	-32.1
803	15.8	47	66	16.3	43.1	-34.6
821	15.0	48	65	15.6	41.6	-34.5

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- P band power amplifier
- All 4G/5G cellular application within 0.5 to 1GHz

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+110	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	$R_{\theta JC}$	1.2	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

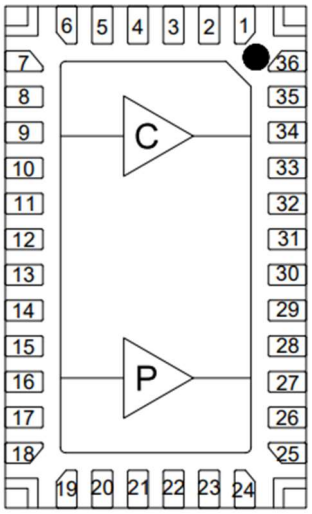
Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0, I_{DS}=100uA	$V_{(BR)DSS}$		110		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 90V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 11 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS(th)}$	——	2	——	V
Gate Quiescent Voltage (V_{DD} = 50V, I_D = 55mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.36	——	V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 50Vdc, I_{DQ} = 55mA, f = 800 MHz

VSWR 10:1 at 50W pulse CW Output Power	No Device Degradation

Figure 1: Pin Connection definition

Transparent top view (Backside grounding for source)



Pin No.	Symbol	Description
9,10	RF IN/Vgs1	RF Input, Vgs bias for main path
14,15,16	RF IN/Vgs2	RF Input, Vgs bias for peak path
33,34	RF OUT/VDD1	RF Output, VDD bias for Main path
27,28,29	RF OUT/VDD2	RF Output, VDD bias for Peak path
Rest pins	NC	No connection
2,5,7,12,13,18,20,23,25,30,31,36, Package Base	GND	DC/RF Ground. Must be soldered directly to heatsink or copper coin for CW application.

758-821MHz application board

Reference Circuit of Test Fixture Assembly Diagram
20mils RO4350B

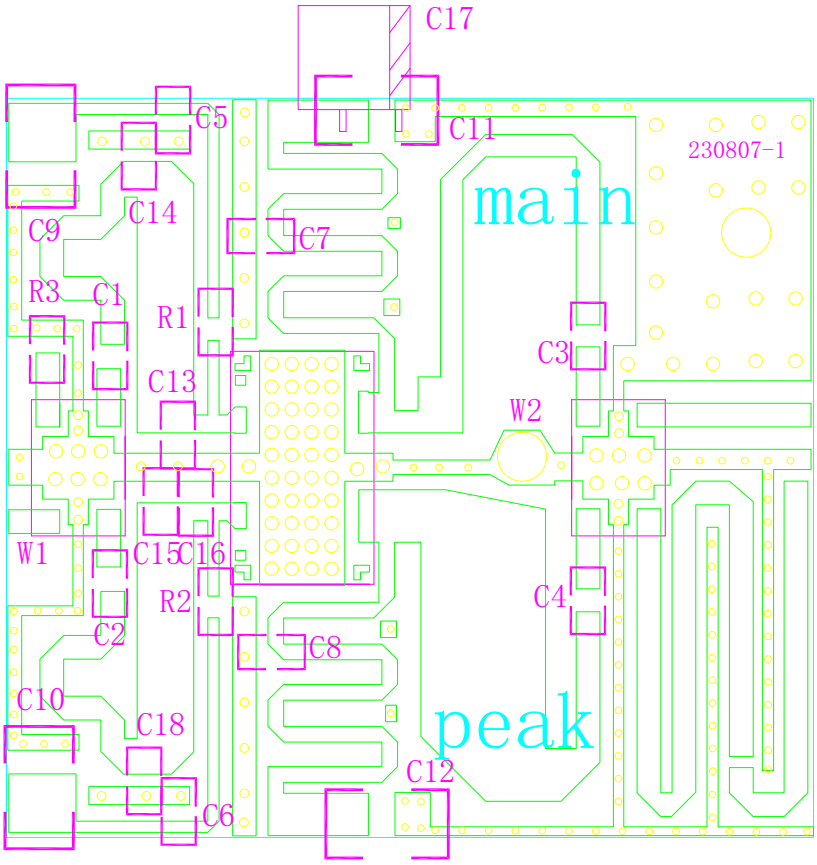


Figure 2. Test Circuit Component Layout

Table 5. Test Circuit Component Designations and Values

Designator	Comment	Footprint	Quantity
C1, C2, C3, C4, C5, C6, C7, C8	100pF/250V	0603	8
C9, C10, C11, C12	10uF/100V	1210	4
C13, C15	12pF/250V	0603	2
C14	6.8pF/250V	0603	1
C16	2.2pF/250V	0603	1
C17	100uF/63V		1
C18	8.2pF/250V	0603	1
R1, R2	10 Ω	0603	2
R3	51 Ω	0805	1
W1, w2	HC07F03		2

TYPICAL CHARACTERISTICS

Figure 5. Power Gain and Drain Efficiency as function of Power Output at Idq=160mA

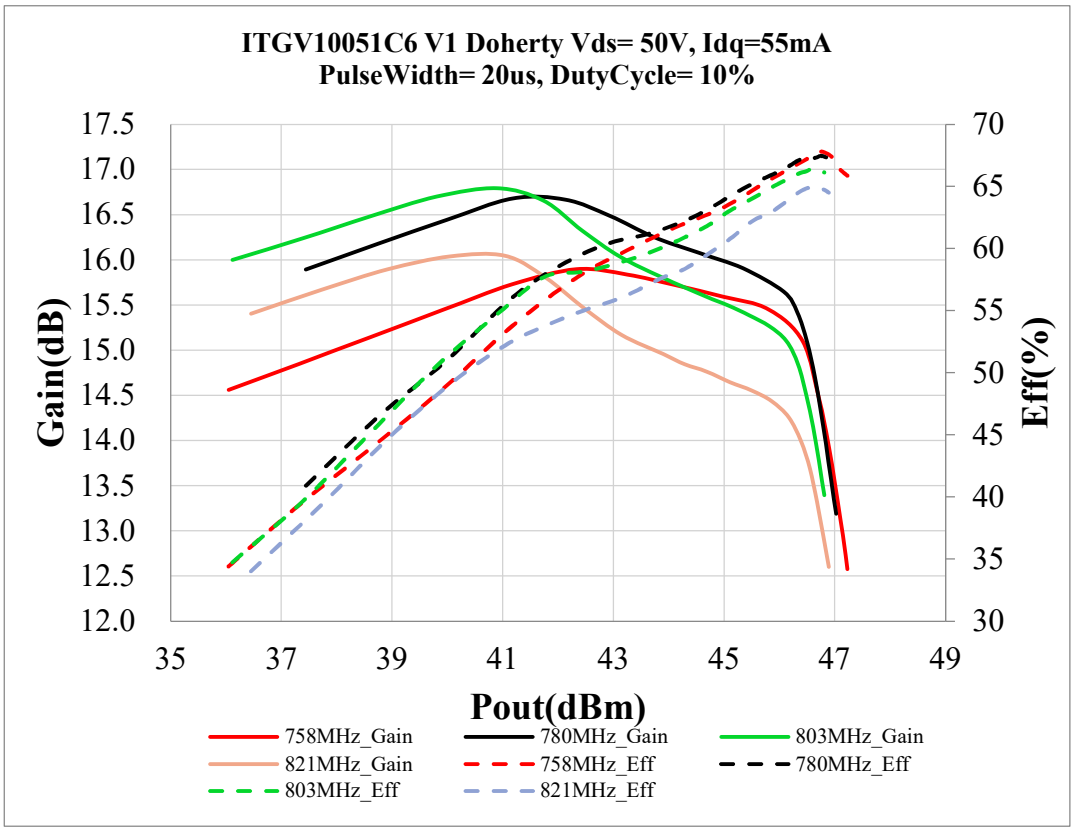
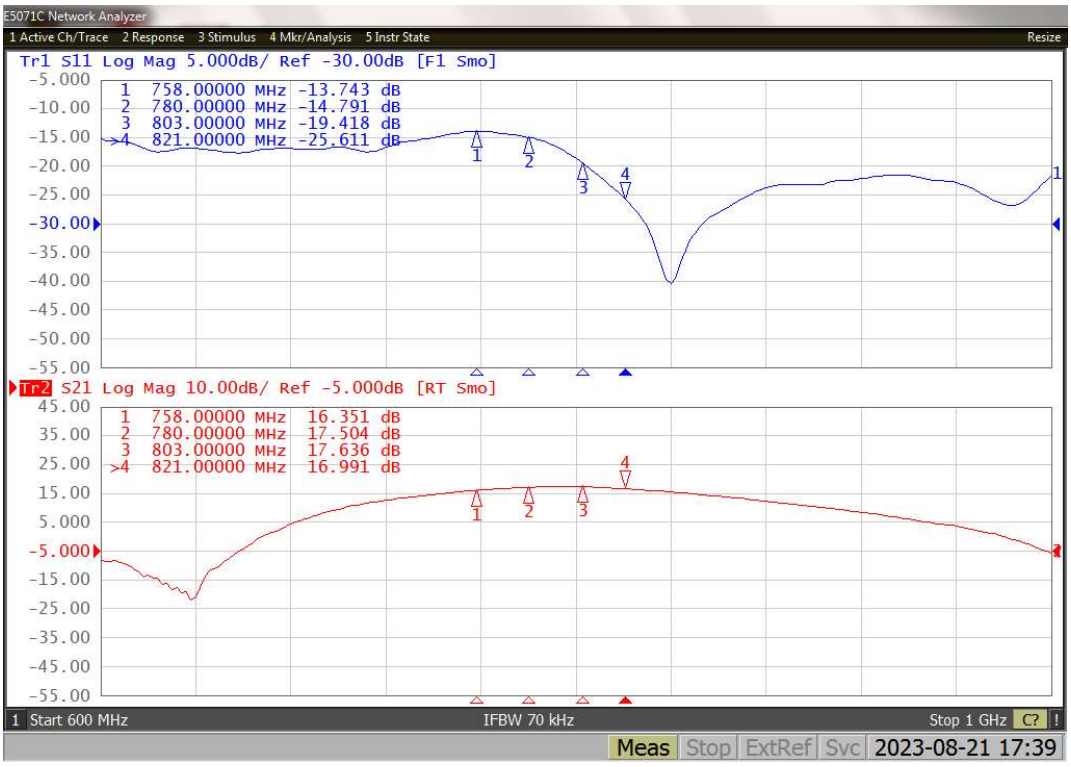
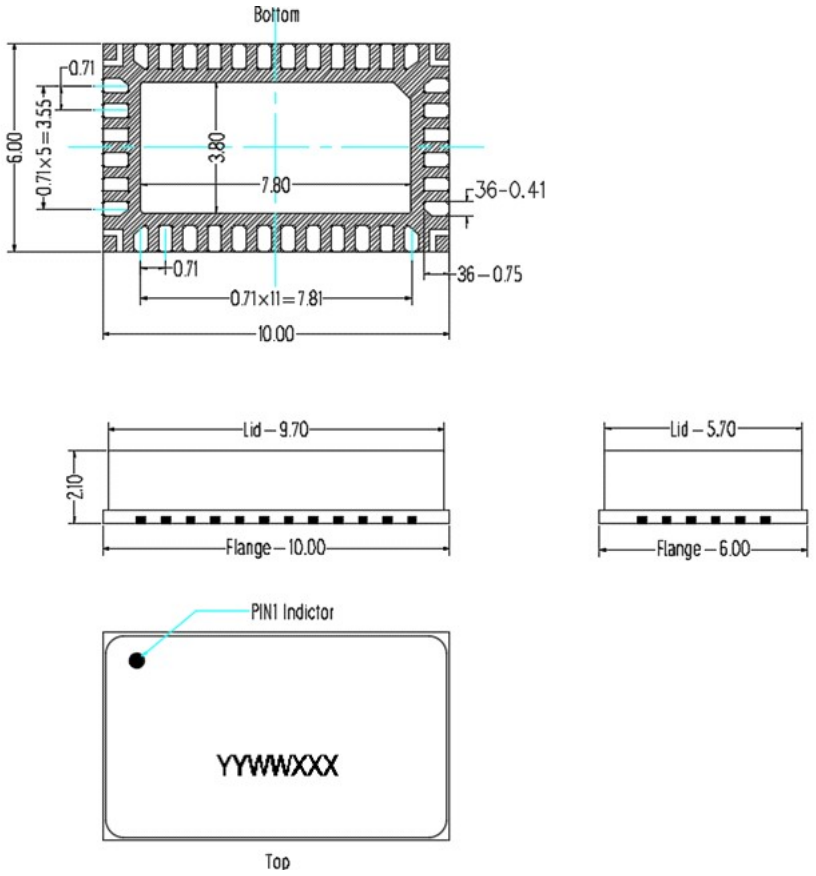


Figure 5.Network analyzer output S11/S21



Package Dimensions

10*6 Plastic Package



Notes:

1. All dimensions are in mm;
2. The tolerances unless specified are ±0.2mm.

Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2023/8/22	**Rev 1.0**	**Preliminary Datasheet**

Application data based on LSM-23-27

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