



GaN HEMT 50V, 130W, 1.8-2.7GHz Power Transistor



Description

The STAV27130C6 is a dual path 130W, internal matched GaN HEMT, operated from 1.8-2.7GHz. It features high gain, high efficiency, wide band and low cost, in 10*6mm open cavity plastic package. It can be configured as a single stage Doherty capable of delivering Pavg of 20W.

There is no guarantee of performance when this part is used outside of stated frequencies.

➤ Typical Doherty Single--Carrier W--CDMA Characterization Performance at 2.6GHz:

Input Signal :WCDMA 1 Carrier with PAR = 10 dB @ 0.01% Probability on CCDF , Pulsed CW: 20us, 10%
VDD = 50 Vdc, IDQA = 150mA, VGSB = -5.0Vdc,

Freq (GHz)	Pavg=38dBm WCDMA Signal			Pavg=43dBm WCDMA Signal		
	Gp (dB)	Eff (%)	ACPR5M (dBc)	Gp (dB)	Eff (%)	ACPR5M (dBc)
2.5	16.01	34.62	-40.46	14.87	56.43	-31.17
2.6	16.27	37.00	-40.06	14.93	57.61	-32.30
2.7	15.73	37.45	-41.59	14.54	56.19	-36.29

Applications

- 5G Doherty amplifier within 2.5-2.7, 2.1-2.2, 1.8-1.9G either as driver or as final
- S band power amplifier
- L band power amplifier

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

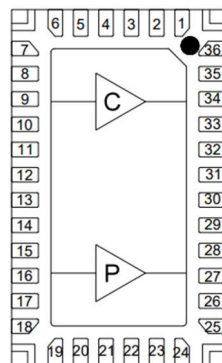
1. Set VGS to the pinch--off (VP) voltage, typically -5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically -5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Figure 1: Pin Connection definition

Transparent top view (Backside grounding for source)



Pin No.	Symbol	Description
9,10	RF IN/Vgs1	RF Input, Vgs bias for main path
15,16	RF IN/Vgs2	RF Input, Vgs bias for peak path



33,34	RF OUT/VDD1	RF Output, VDD bias for Main path
27,28	RF OUT/VDD2	RF Output, VDD bias for Peak path
Rest pins	NC	No connection
2,5,7,12,13,18,20,23,25,30,31,36, Package Base	GND	DC/RF Ground. Must be soldered directly to heatsink or copper coin for CW application.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum gate current	I_{gs}	9	mA
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA $T_c = 85^\circ\text{C}$, $P_{diss} = 15\text{W}$ at $P_{avg} = 43\text{dBm}$ WCDMA 1 carrier	$R_{\theta JC}$	2.3	°C /W

Notes: Based on expected carrier amplifier efficiency of Doherty, P_{avg} assumes 10% peaking amplifier contribution of total average Doherty rated power. Thermal resistance is measured to package backside

Table 3. Electrical Characteristics (TA = 25°C unless otherwise noted)

DC Characteristics (main path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = -8\text{V}$; $I_{DS} = 7.5\text{mA}$	V_{DSS}		200		V
Gate Threshold Voltage	$V_{DS} = 10\text{V}$, $I_D = 7.5\text{mA}$	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	$V_{DS} = 50\text{V}$, $I_{DS} = 60\text{mA}$, Measured in Functional Test	$V_{GS(Q)}$		-3.1		V

DC Characteristics (peak path, measured on wafer prior to packaging)

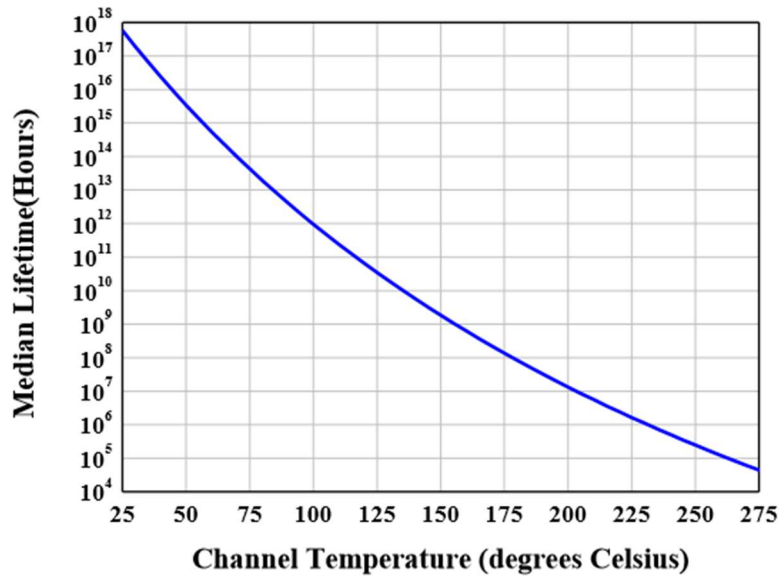
Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = -8\text{V}$; $I_{DS} = 7.5\text{mA}$	V_{DSS}		200		V
Gate Threshold Voltage	$V_{DS} = 10\text{V}$, $I_D = 7.5\text{mA}$	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	$V_{DS} = 50\text{V}$, $I_{DS} = 60\text{mA}$, Measured in Functional Test	$V_{GS(Q)}$		-3.1		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	2.6GHz, $P_{out} = 42\text{dBm}$ WCDMA 1 Carrier, All phase, No device damages	VSWR		10:1		

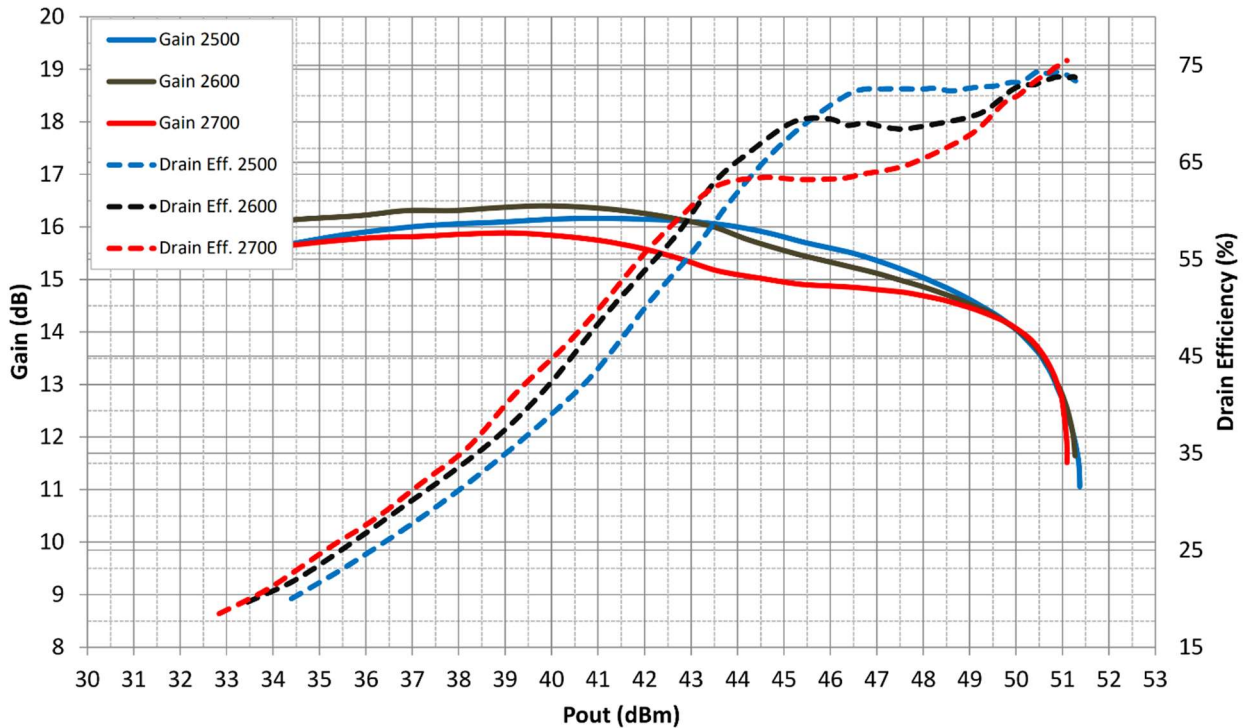


Figure 2: Median Lifetime vs. Channel Temperature



Typical performance
2500-2700MHz Doherty

Figure 3: Efficiency and power gain as function of Pout (2.5-2.7GHz Doherty)



Freq (MHz)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)	P1dB Gain(dB)	P5dB (dBm)	P5dB (W)	P5dB Eff(%)
2500	50.78	119.81	74.16	15.06	51.37	137.21	73.12
2600	50.78	119.56	73.65	15.34	51.27	133.94	73.77
2700	50.99	125.65	75.16	14.87	51.10	128.71	75.48



Figure 4: Network analyzer output, S11 and S21 (2.5-2.7GHz Doherty)

m1 freq=2.500 GHz dB(S(2,1))=16.096 dB(S(1,1))=-19.174	m2 freq=2.600 GHz dB(S(2,1))=16.537 dB(S(1,1))=-16.152	m3 freq=2.700 GHz dB(S(2,1))=16.182 dB(S(1,1))=-13.952
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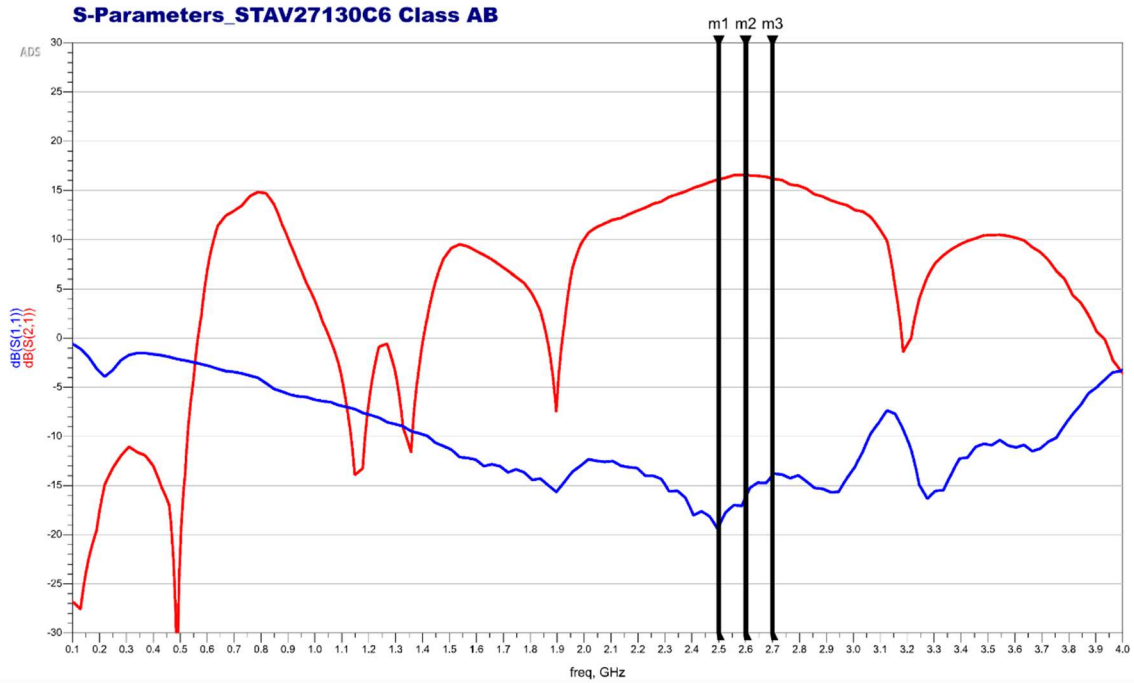
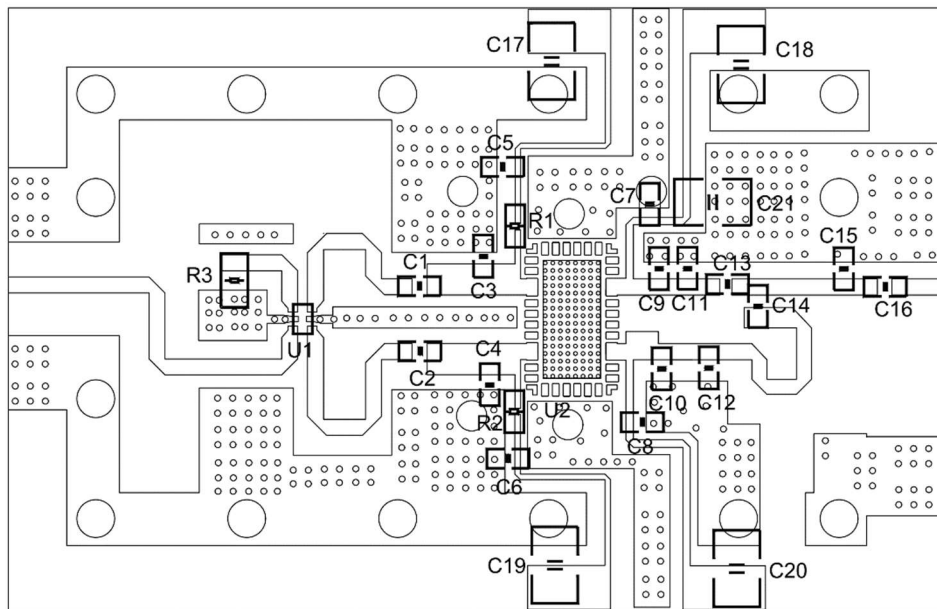


Figure 5: Picture of application board Doherty circuit for 2.5-2.7GHz





Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2023/8/22	V1.0	Preliminary Datasheet Creation

Application data based on: ZBB-23-25

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