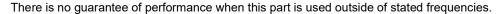
GaN HEMT 50V, 100W, 1.8-2.7GHz Power Transistor

Description

The STAV27100C6 is a dual path 100W, internal matched GaN HEMT, operated from 1.8-2.7GHz. It features high gain, high efficiency, wide band and low cost, in 10*6mm open cavity plastic package. It can be configured as a single stage Doherty capable of delivering Pavg of 16W.



- Typical Doherty Single--Carrier W--CDMA Characterization Performance
 Input Signal :WCDMA 1 Carrier with PAR = 10 dB @ 0.01% Probability on CCDF, Pulsed CW: 20us, 10%
- VDD = 50 Vdc, IDQA = 45 mA, VGSB = −5.0Vdc,

Freq	Pulse CW Signal			Pavg=42dBm WCDMA Signal		
(GHz)	P1-Gain	Psat	Psat	Gp (dB)	Eff (%)	ACPR5M (dBc)
(OHZ)	(dB)	(dBm)	(W)	- Gp (uв)	□ □ (70)	ACPRSIVI (dBc)
2.5	14.16	50.08	101.7	14.20	59.86	-27.95
2.6	14.89	50.01	101.2	14.75	60.46	-29.67
2.7	15.04	50.07	101.6	15.07	59.55	-32.22

VDD = 50 Vdc, IDQA = 45 mA, VGSB = −5.0Vdc,

Freq	Pι	ılse CW Signa	il	Pavg=42dBm WCDMA Signal		
(GHz)	P1-Gain	Psat	Psat	Gp (dB)	Eff (%)	ACPR5M (dBc)
(0112)	(dB)	(dBm)	(W)	- Gp (uв)	EII (70)	ACPRSIVI (dBC)
2.3	15.07	50.77	119.32	15.14	59.95	-27.42
2.35	15.12	50.82	120.89	15.10	60.50	-28.83
2.4	15.11	50.64	115.86	14.91	59.46	-30.75

Applications

- 5G Doherty amplifier within 2.5-2.7,2.3-2.4, 2.1-2.2, 1.8-1.9G either as driver or as final
- S band power amplifier
- L band power amplifier

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

- 1. Set VGS to the pinch--off (VP) voltage, typically -5 V
- 2. Turn on VDS to nominal supply voltage
- 3. Increase VGS until IDS current is attained
- 4. Apply RF input power to desired level

Turning the device OFF

- 1. Turn RF power off
- 2. Reduce VGS down to VP, typically -5 V
- 3. Reduce VDS down to 0 V
- 4. Turn off VGS

Figure 1: Pin Connection definition

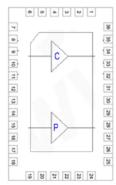
Transparent top view (Backside grounding for source)

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Pin No.	Symbol	Description
9,10	RF IN/Vgs1	RF Input, Vgs bias for main path
15,16	RF IN/Vgs2	RF Input, Vgs bias for peak path
33,34	RF OUT/VDD1	RF Output, VDD bias for Main path
27,28	RF OUT/VDD2	RF Output, VDD bias for Peak path
Rest pins	NC	No connection
2,5,7,12,13,18,20,23,25,30,31,36,	OND	DC/RF Ground. Must be soldered directly to heatsink or copper coin for
Package Base	GND	CW application.

Table 1. Maximum Ratings

_			
Rating	Symbol	Value	Unit
DrainSource Voltage	V _{DSS}	+200	Vdc
GateSource Voltage	V _{GS}	-8 to +0.5	Vdc
Operating Voltage	V _{DD}	55	Vdc
Maximum gate current	lgs	9	mA
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T _C	+150	°C
Operating Junction Temperature	T _J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit	
Thermal Resistance, Junction to Case by FEA	Rejc	2.5	9C /W	
T _C = 85°C, Pdiss=10.5W at Pavg=42dBm WCDMA 1 carrier	Kejc	2.5	°C /W	

Notes: Based on expected carrier amplifier efficiency of Doherty, Pavg assumes 10% peaking amplifier contribution of total average Doherty rated power. Thermal resistance is measured to package backside

Table 3. Electrical Characteristics (TA = 25℃ unless otherwise noted)

DC Characteristics (main path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol Min Typ		Max	Unit	
Drain-Source Breakdown Voltage	VGS=-8V; IDS=5mA	V _{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 5mA	V _{GS(th)} -4 -2		-2	V	
Gate Quiescent Voltage	VDS =50V, IDS=45mA, Measured in Functional Test	V _{GS(Q)} -3.1		-3.1		V

DC Characteristics (peak path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Тур	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=7.5mA	V _{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 7.5mA	$V_{GS(th)}$	-4		-2	V



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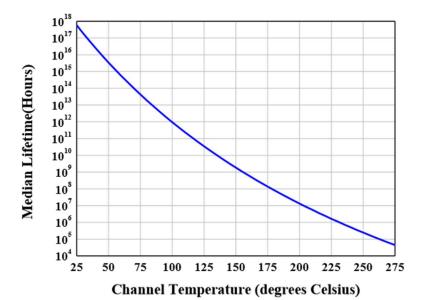
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Gate Quiescent Voltage	VDS =50V, IDS=60mA, Measured in Functional Test	$V_{GS(Q)}$		-3.1		V
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Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Тур	Max	Unit
Load mismatch capability	2.6GHz, Pout=42dBm WCDMA					
	1 Carrier, All phase,	VSWR		10:1		
	No device damages					

Figure 2: Median Lifetime vs. Channel Temperature





Typical performance 2500-2700MHz Doherty

Figure 3: Efficiency and power gain as function of Pout (2.5-2.7GHz Doherty)

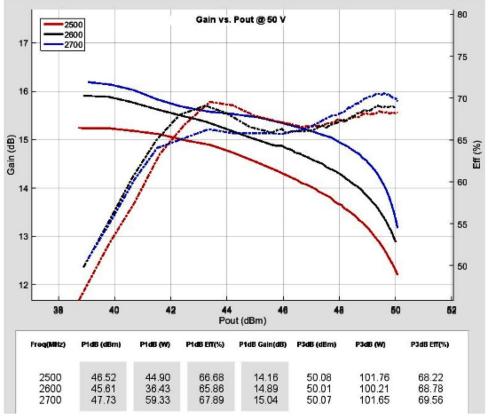


Figure 4: Network analyzer output, S11 and S21 (2.5-2.7GHz Doherty)

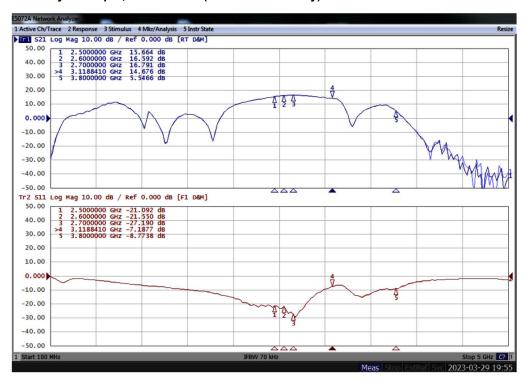


Figure 5: Picture of application board Doherty circuit for 2.5-2.7GHz

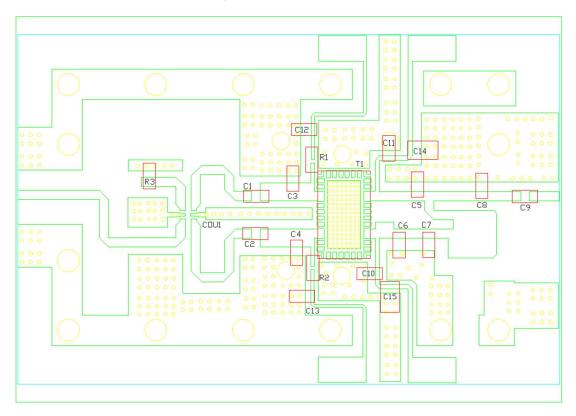


Table 4. Bill of materials of application board (PCB layout upon request, RO4350B 20mils)

Part	Quantity	Description	Part Number	Manufacture
C1,C2,C9,C10,C11,C12,C13	7	10pFHigh Q	251SHS100BSE	TEMEX
		Capacitor		
C3,C4	2	1.2pFHigh Q	251SHS1R2BSE	TEMEX
		Capacitor		
C5	1	1.5pFHigh Q	251SHS1R5BSE	TEMEX
		Capacitor		
C15,C14	2	10uF MLCC	RS80R2A106M	MARUWA
C6	1	2.0pFHigh Q	251SHS2R0BSE	TEMEX
		Capacitor		
C8	1	1.1pFHigh Q	251SHS1R1BSE	TEMEX
		Capacitor		
C7,	1	0.3pFHigh Q	251SHS0R3BSE	TEMEX
		Capacitor		
R1,R2	2	10 Ω Power Resistor	ESR03EZPF100	ROHM
R3	1	51 Ω Power Resistor	ESR03EZPF510	ROHM
COU1	1	3dB bridge	C2327J50503AHF	ANAREN
T1	1	100W GaN	STAV27100C6	Innogration



Typical performance 2300-2400MHz Doherty

Figure 6: Efficiency and power gain as function of Pout

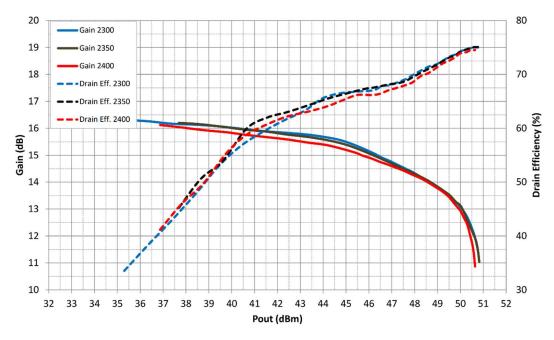


Figure 7: Network analyzer output, S11 and S21





Figure 8: Picture of application board Doherty circuit

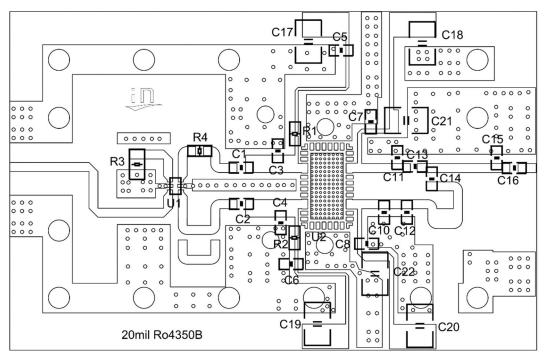


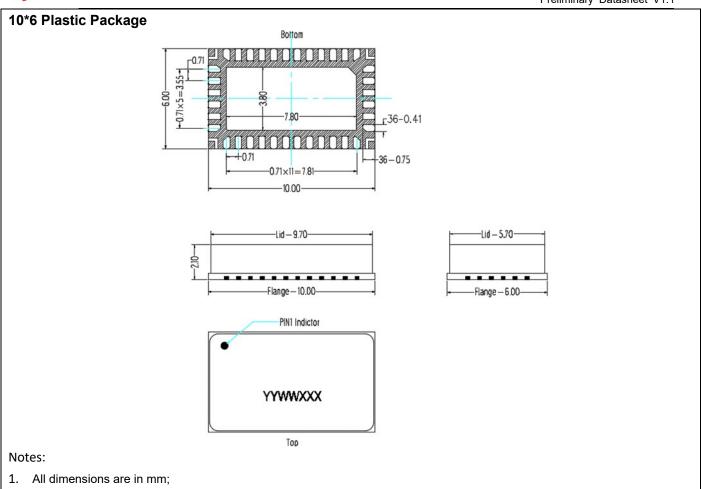
Table 5. Bill of materials of application board (PCB layout upon request, RO4350B 20mils)

Reference	Footprint	Value	Quantity
C1, C2, C5, C6, C7, C8,	0603	10.5[/250]/	9
C13, C14, C16	0603	10pF/250V	9
C3, C10	0603	1.0pF/250V	2
C4, C12	0603	1.6pF/250V	2
C11	0603	1.5pF/250V	1
C15	0603	1.2pF/250V	1
C17, C18, C19, C20,	1210	10F/100V	6
C21, C22	1210	10uF/100V	6
R1, R2	0603	10R	2
R3	1206	50R	1
R4	0805	9.1R	1
U1	0805	C2327J5003AHF	1
U2	C6	STAV27100C6	1



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2. The tolerances unless specified are ±0.2mm.

Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2023/3/30	V1.0	Preliminary Datasheet Creation
2023/12/2	V1.1	Add 2.3-2.4G application data

Application data based on: LWH-23-06/ZBB-23-36

Notice

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