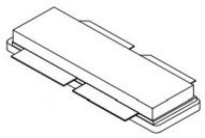
2.4-2.5Hz, 32V 300W, High Power RF LDMOS FETs

ITCH25280D4



Description

The ITCH25280D4 is a 300-watt, internally matched LDMOS FETs, designed for Multiple use especially RF Energy application including cooking, heating and medical with frequencies from 2400 to 2500 MHz.

- Typical Performance (on Innogration fixture with device soldered): Tcase=25 Degree C

Freq	P1dB	P1dB	P1dB Eff	P1dB Gain	P3dB	P3dB	P3dB Eff
(MHz)	(dBm)	(W)	%	dB	(dBm)	(W)	%
2400	55.39	345.87	58.47	15.26	55.74	375.12	59
2450	55.20	331.08	58.21	15.48	55.59	362.56	58.5
2500	54.60	288.47	56.74	15.62	55.27	336.52	58

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	70	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case Tcase= 85°C, Pout=300W CW	$R_{\theta JC}$	0.2	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Breakdown Voltage (V_{GS}=0V; I_D=100uA)	V_{DSS}	65	——	——	V

Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	——	——	10	μA
Gate--Source Leakage Current (V_{GS} = 6 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 600 uA)	$V_{GS(th)}$	——	1.6	——	V
Gate Quiescent Voltage (V_{DD} = 32 V, I_{DQ} = 20 mA, Measured in Functional Test)	$V_{GS(Q)}$		2.25		V

Functional Tests (In Innogration Test Fixture, 50 ohm system) :V_{DD} = 32 Vdc, I_{DQ} = 20 mA, f = 2450 MHz, CW Signal Measurements., Pin=12W,

Power Gain	Gp	——	14	——	dB
Drain Efficiency@Pout	η_D	——	58	——	%
Output Power	P_{-3dB}	300		——	W
Input Return Loss	IRL	——	-7	——	dB

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 32 Vdc, I_{DQ} = 20 mA, f = 2450MHz

VSWR 10:1 at 300W pulse CW Output Power	No Device Degradation

Figure 1

Signal: Pulse width20us, duty cycle 10%

Vgs= 2.25V,Vds= 32V,Idq=20mA

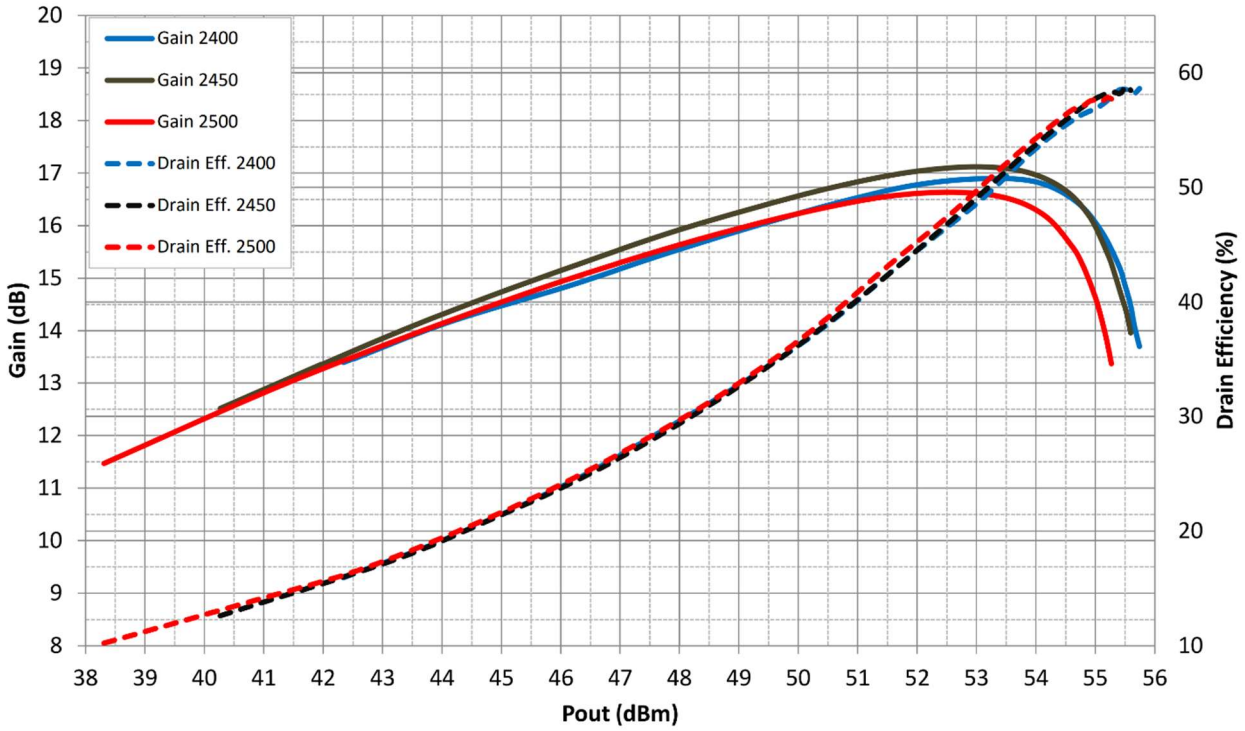
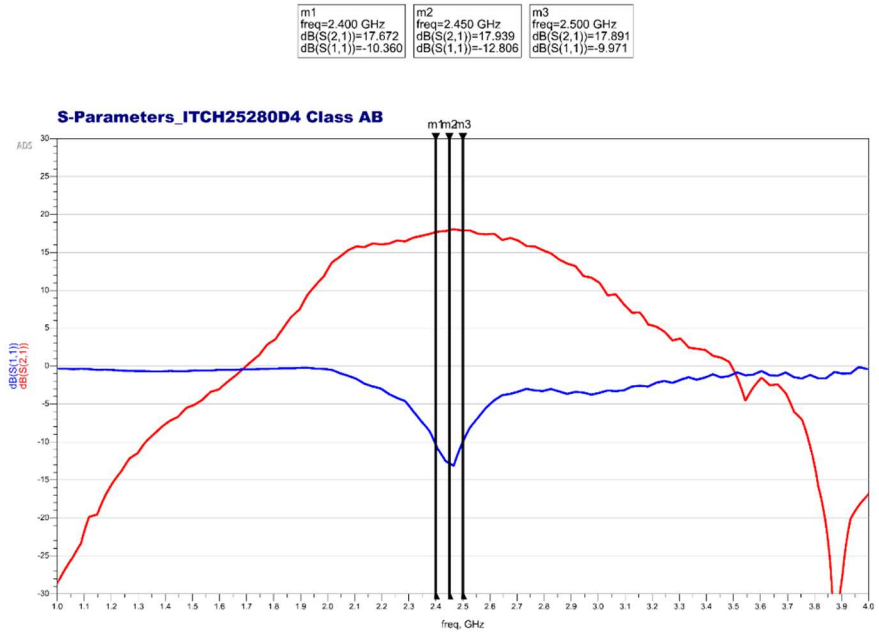


Figure 3. Network analyzer output S11/S21 (Vdd=32V, Idq=1500mA)



Reference Circuit of Test Fixture Assembly Diagram

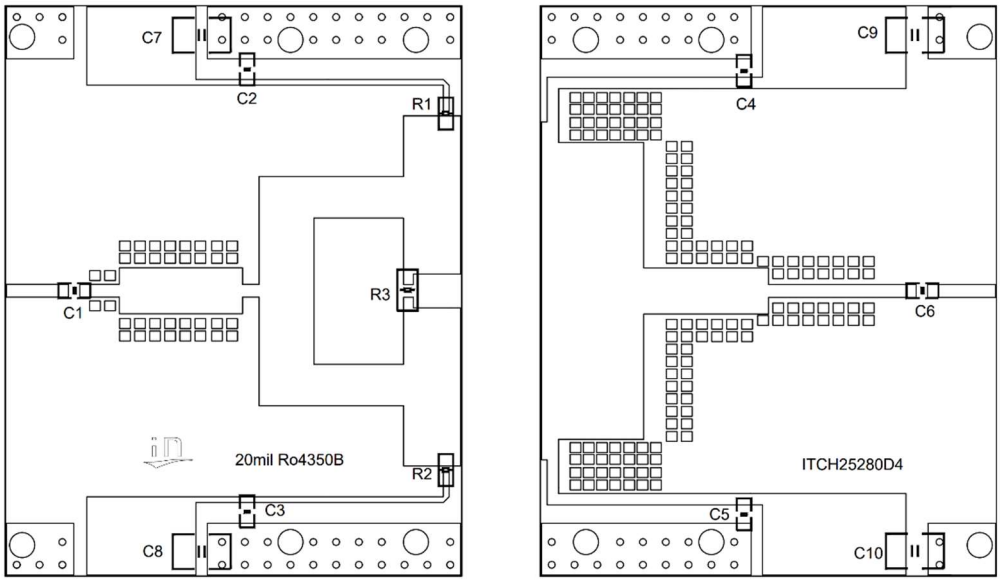


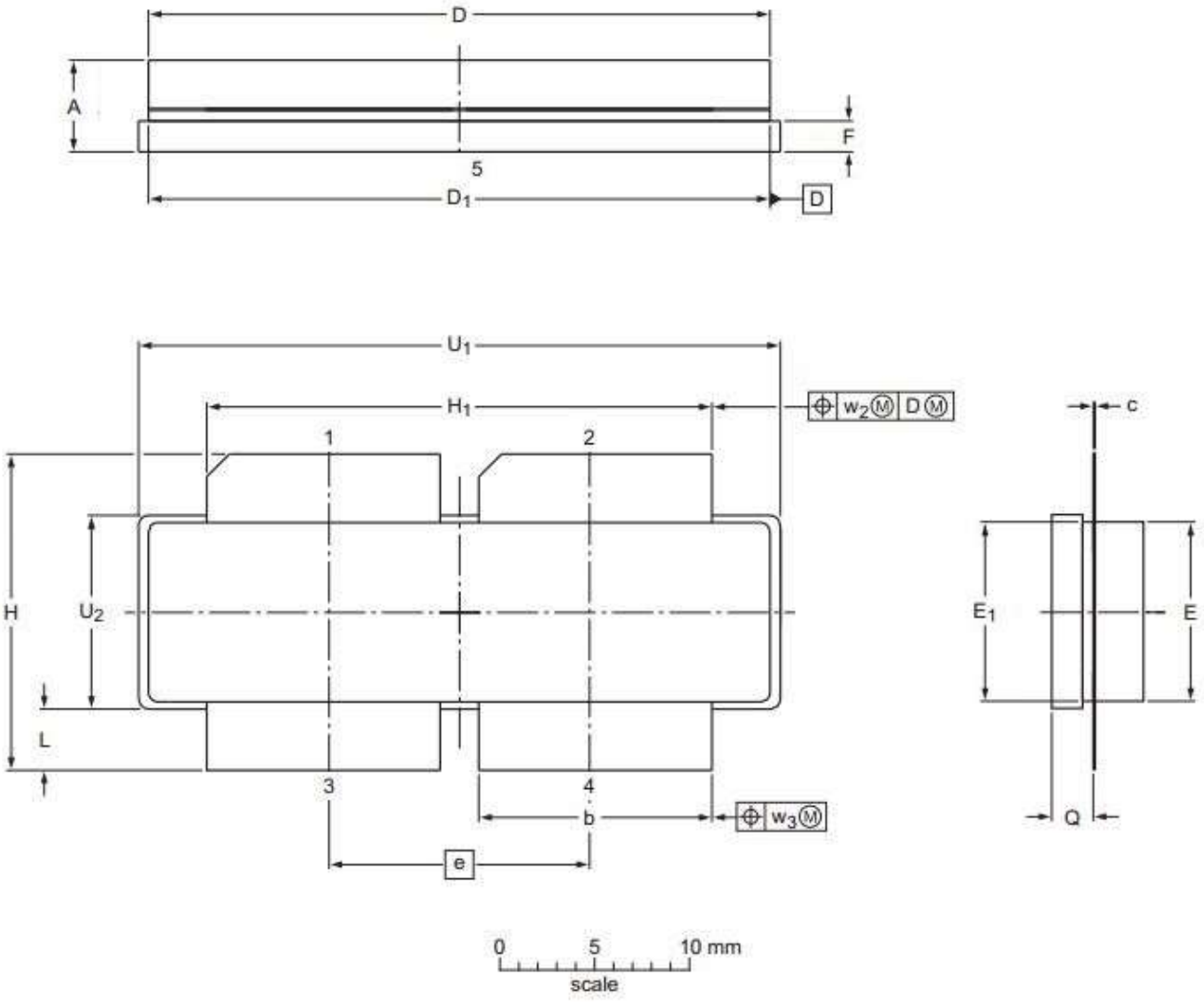
Figure 1. Test Circuit Component Layout

Table 1. Test Circuit Component Designations and Values

Reference	Footprint	Value	Quantity
C1, C2, C3, C4, C5, C6	0603	8.2pF/250V	6
R1, R2	0603	10R	2
R3	1206	10R	1
C7, C8, C9, C10	1210	10uF/100V	4
U1	D4	ITCH25280D4	1

Package Outline

Earless flanged ceramic package; 4 leads（1、2—DRAIN、3、4—GATE、5—SOURCE）



UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	Q	U_1	U_2	W_2	W_2
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	2.26 2.01	32.39 32.13	10.29 10.03	0.25	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.089 0.079	1.275 1.265	0.405 0.395	0.01	0.01

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4					03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2023/9/27	**V1**	**Preliminary Datasheet Creation**

Application data based on ZBB-23-31

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