



GaN HEMT 50V, 200W, 4.4-5GHz RF Power Transistor

Description

The STCV50201L4 is a dual path 200watt, GaN HEMT, ideal for applications from 4.4 to 5GHz. It can be configured as asymmetrical Doherty for 5G application, delivering 25W average power according to normal 8.5dB back off.

It is housed in 15*5.5mm ceramic package with high thermally conductive flange.

There is no guarantee of performance when this part is used outside of stated frequencies.

- Typical RF performance on application board with device soldered

VDS = 48 V, Idq_main = 130 mA, Vgs_peak = -5.6V

STCV50201L4



Freq (GHz)	Pulse CW Signal ⁽¹⁾			P _{avg} =44.5dBm WCDMA Signal ⁽²⁾		
	P1-Gain (dB)	P3 (dBm)	P3 (W)	Gp (dB)	η _D (%)	ACPR _{5M} (dBc)
4.40	10.96	53.29	213	11.24	39.88	-30.89
4.50	11.32	53.10	204	11.43	39.60	-35.87
4.60	11.89	53.09	203	11.86	41.99	-38.94
4.70	11.83	53.06	203	11.95	44.20	-36.74
4.80	12.11	52.99	200	11.66	44.09	-33.70
4.90	11.72	53.23	210	11.13	42.15	-32.32
5.00	10.30	53.35	216	10.60	39.80	-29.38

(1) Pulsed condition: 20us and 10%,

(2) 1C WCDMA; Signal PAR = 10 dB @ 0.01% Probability on CCDF.

Applications

- N79 Doherty amplifier
- C band power amplifier application

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch-off (VP) voltage, typically -5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically -5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Figure 1: Pin Connection definition

Transparent top view (Backside grounding for source)

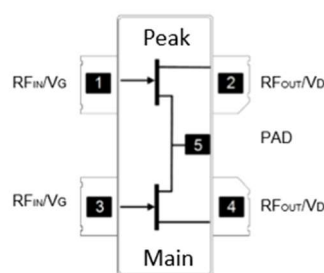




Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum gate current	I_{gs}	27	mA
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA $T_c = 85^\circ\text{C}$, at $P_{out} = 25\text{W WCDMA}$	$R_{\theta JC}$	2.4	°C /W

Table 3. Electrical Characteristics (TA = 25°C unless otherwise noted)

DC Characteristics (main path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = -8\text{V}$; $I_{DS} = 10\text{mA}$	V_{DSS}		200		V
Gate Threshold Voltage	$V_{DS} = 10\text{V}$, $I_D = 10\text{mA}$	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	$V_{DS} = 50\text{V}$, $I_{DS} = 110\text{mA}$, Measured in Functional Test	$V_{GS(Q)}$		-3.1		V

DC Characteristics (peak path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = -8\text{V}$; $I_{DS} = 17\text{mA}$	V_{DSS}		200		V
Gate Threshold Voltage	$V_{DS} = 10\text{V}$, $I_D = 17\text{mA}$	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	$V_{DS} = 50\text{V}$, $I_{DS} = 130\text{mA}$, Measured in Functional Test	$V_{GS(Q)}$		-3.13		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	5GHz, $P_{out} = 25\text{W WCDMA}$ on Doherty All phase, No device damages	VSWR		10:1		



Figure 3: Efficiency and power gain as function of Pout (4.4-5GHz Doherty)

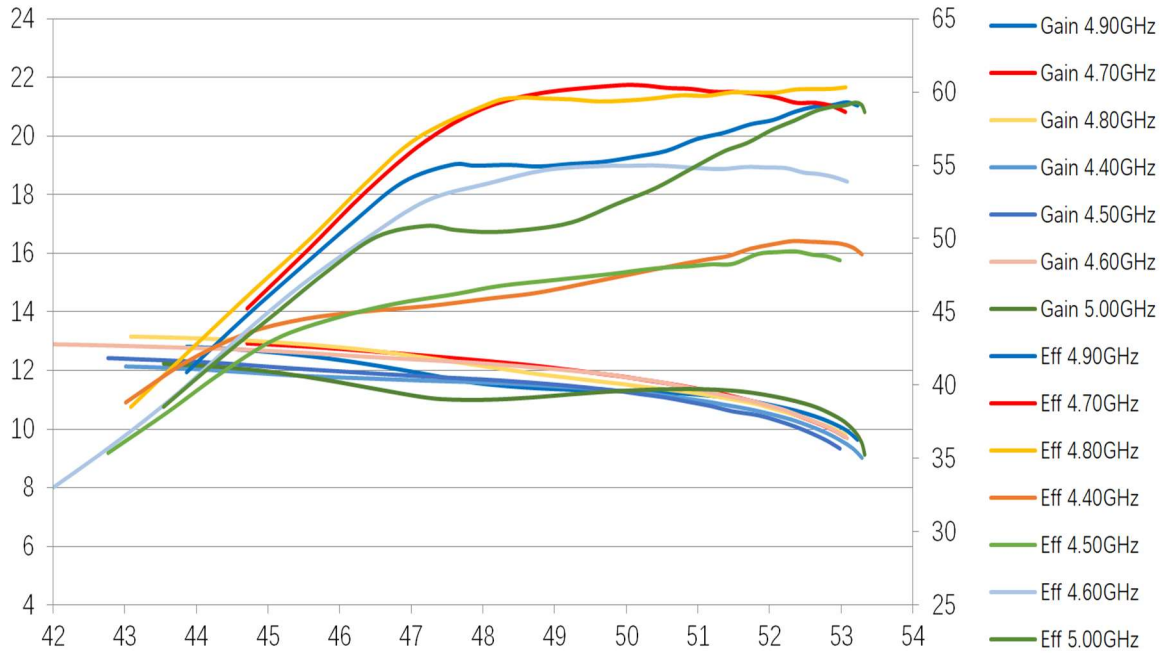


Figure 4: Network analyzer output, S11 and S21 (4.4-5GHz Doherty)

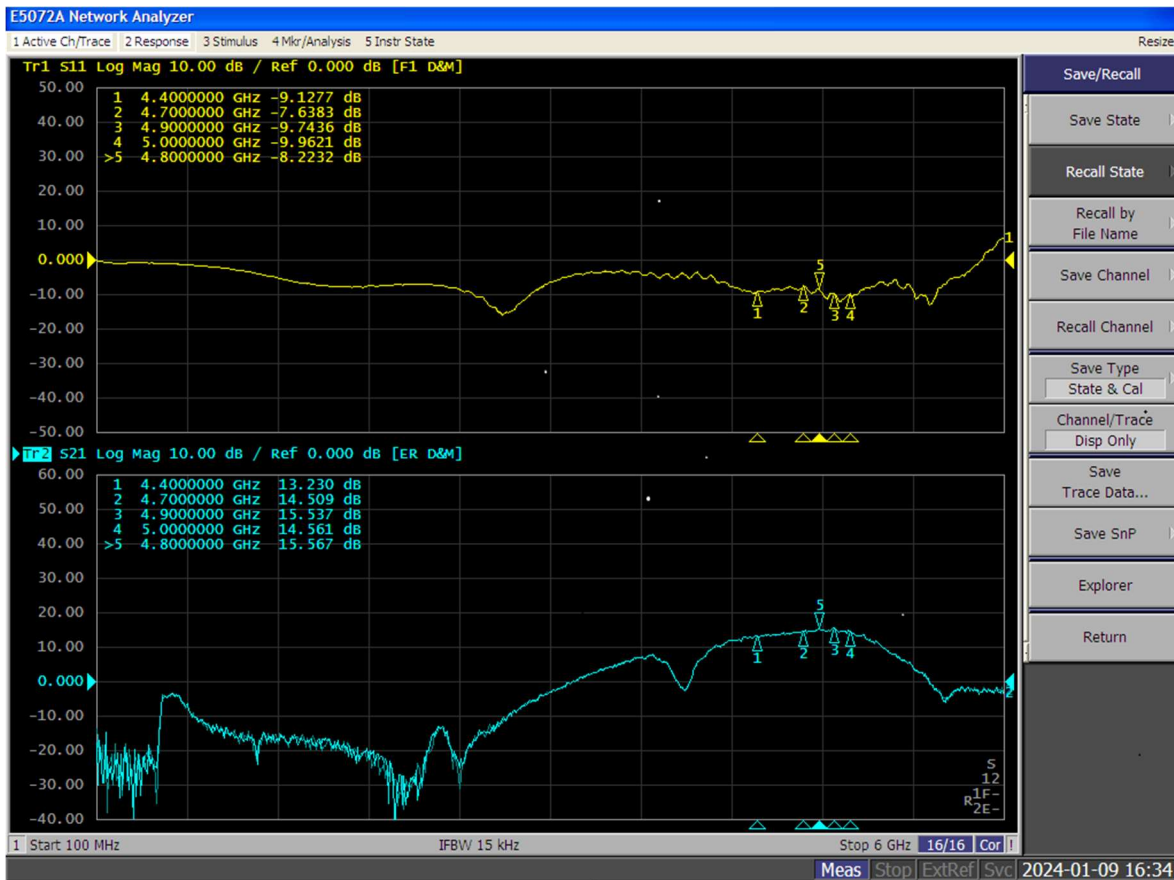


Figure 5: Picture of application board Doherty circuit

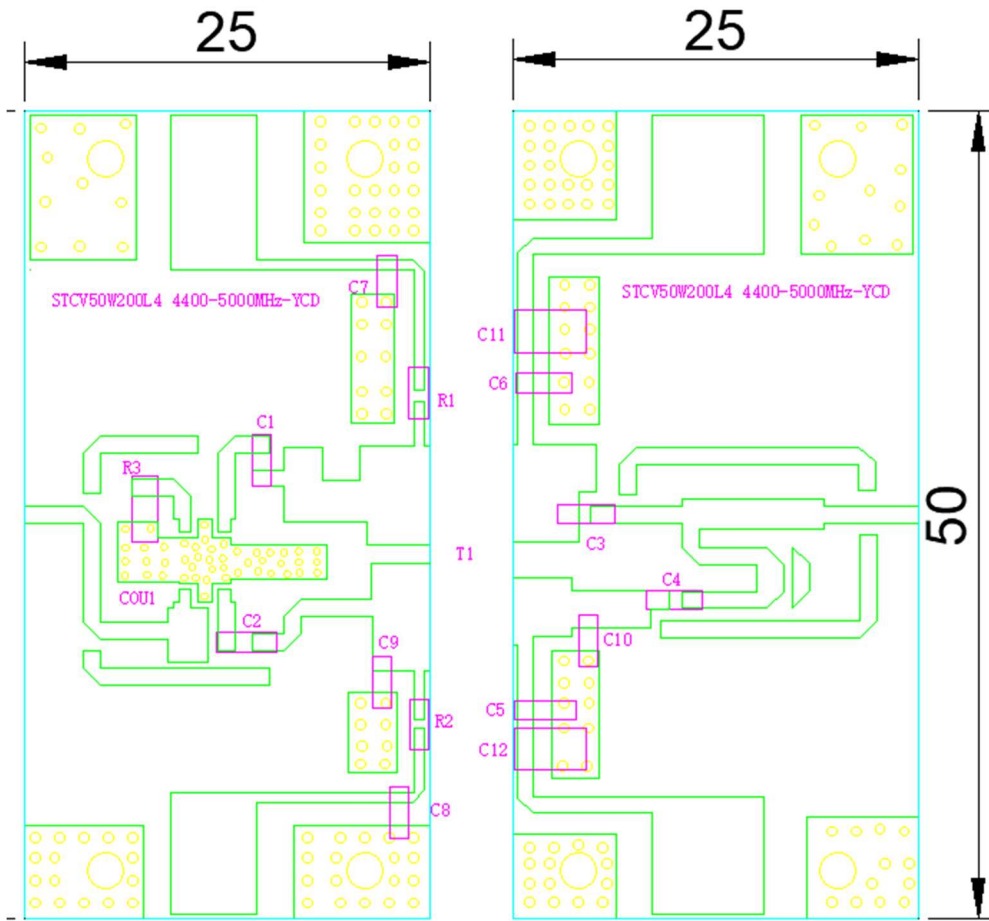
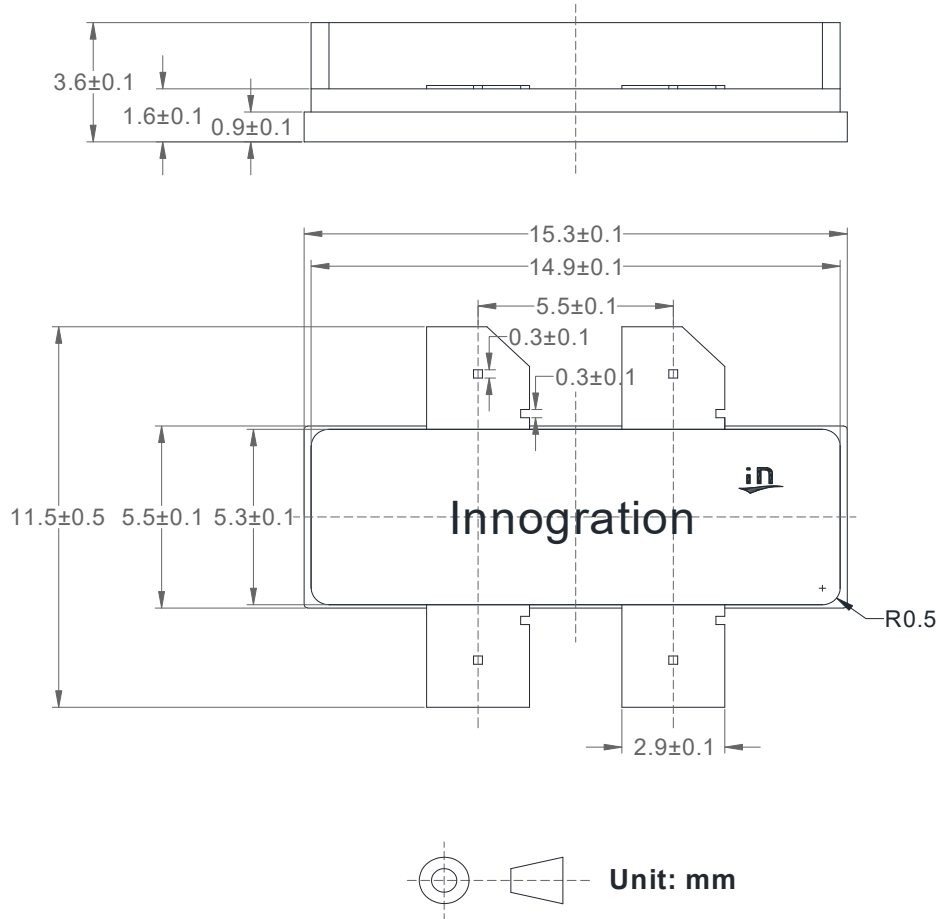


Table 4. Bill of materials of application board (PCB layout upon request, RO4350B 20mils)

C3	1	8.2pF High Q Capacitor	251SHS8R2BSE	TEMEX
C10	1	0.2pF High Q Capacitor	251SHS0R2BSE	TEMEX
C1,C2,C4,C5,C6,C7,C8	7	3.9pF High Q Capacitor	251SHS3R9BSE	TEMEX
C11,C12	2	10uF MLCC	GRM32EC72A106ME05	Murata
C9	1	0.3pF High Q Capacitor	251SHS0R3BSE	TEMEX
R1,R2	2	10 Ω Power Resistor	ESR03EZPF100	ROHM
R3	1	51 Ω Power Resistor	S1206N	RN2
COU1	1	3 dB Bridge	X3C45F1-03S	Anaren
T1	1	200W GaN Dual Transistor	STCV50W201L4	Innogrations



Earless Flanged Ceramic Package; 4 leads



Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2024/1/10	V1.0	Preliminary Datasheet Creation

Application data based on LWH-24-01

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