



# GaN 50V, 900W, 915MHz RF Power Transistor

**STBV101K0RD4**

## Description

The STBV101K0RD4 is a 900W capable, push pull, internally matched GaN HEMT, ideal for ISM or RF energy applications at 915MHz

**In typical CW operation, it can deliver 900W under water cooling condition, and 850W CW under air cooling condition.**

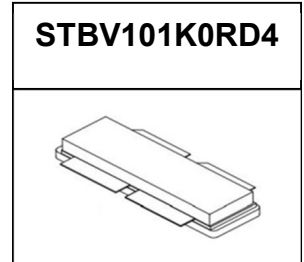
There is no guarantee of performance when this part is used outside of stated frequencies.

- Typical RF performance at 915MHz applications

V<sub>ds</sub>=50V, V<sub>gs</sub>=-4.2V, CW, T<sub>c</sub>=25 degree C

	Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
Water cooling	915	59.09	810.2	79	18.74	59.65	923	82
Air cooling	915	59.08	809.9	78	18.65	59.58	908	80

Recommended driver: ITGV20040J2 (50V LDMOS)



## Applications

- 915MHz RF Energy
- P band power amplifier
- Avionics Power Amplifier

## Important Note: Proper Biasing Sequence for GaN HEMT Transistors

### Turning the device ON

1. Set V<sub>GS</sub> to the pinch-off (V<sub>P</sub>) voltage, typically -5 V
2. Turn on V<sub>DS</sub> to nominal supply voltage
3. Increase V<sub>GS</sub> until I<sub>DS</sub> current is attained
4. Apply RF input power to desired level

### Turning the device OFF

1. Turn RF power off
2. Reduce V<sub>GS</sub> down to V<sub>P</sub>, typically -5 V
3. Reduce V<sub>DS</sub> down to 0 V
4. Turn off V<sub>GS</sub>

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain--Source Voltage	V <sub>DSS</sub>	+200	Vdc
Gate--Source Voltage	V <sub>GS</sub>	-8 to +0.5	Vdc
Operating Voltage	V <sub>DD</sub>	55	Vdc
Maximum gate current	I <sub>gs</sub>	141	mA
Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C
Case Operating Temperature	T <sub>c</sub>	+150	°C
Operating Junction Temperature	T <sub>J</sub>	+225	°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA T <sub>c</sub> = 25°C, at Pd=250W	R <sub>θJC</sub>	0.4	°C /W



Table 3. Electrical Characteristics (TA = 25°C unless otherwise noted)

DC Characteristics (Each path, measured on wafer prior to packaging)

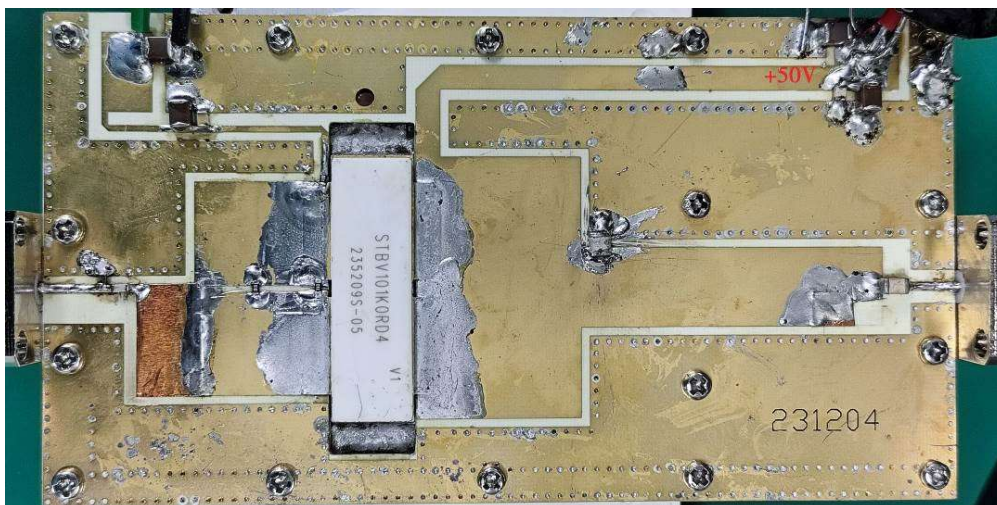
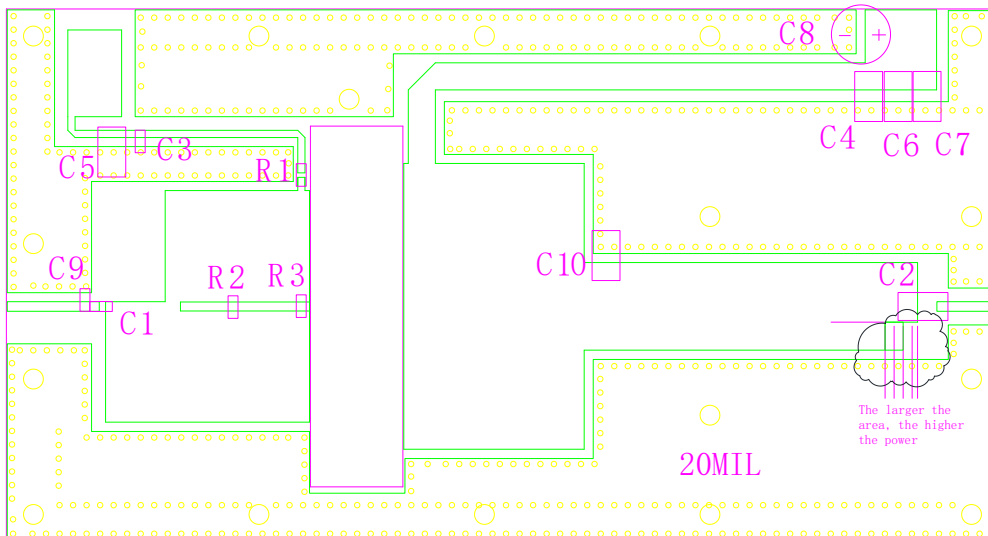
Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=70.5mA	V <sub>DSS</sub>		200		V
Gate Threshold Voltage	VDS =10V, ID = 70.5mA	V <sub>GS(th)</sub>	-4	-	-2	V
Gate Quiescent Voltage	VDS =50V, IDS=500mA, Measured in Functional Test	V <sub>GS(Q)</sub>		--3.3		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	915MHz, Pout=900W pulse CW All phase, No device damages	VSWR		10:1		

Reference Circuit of Test Fixture Assembly Diagram

DXF file upon request

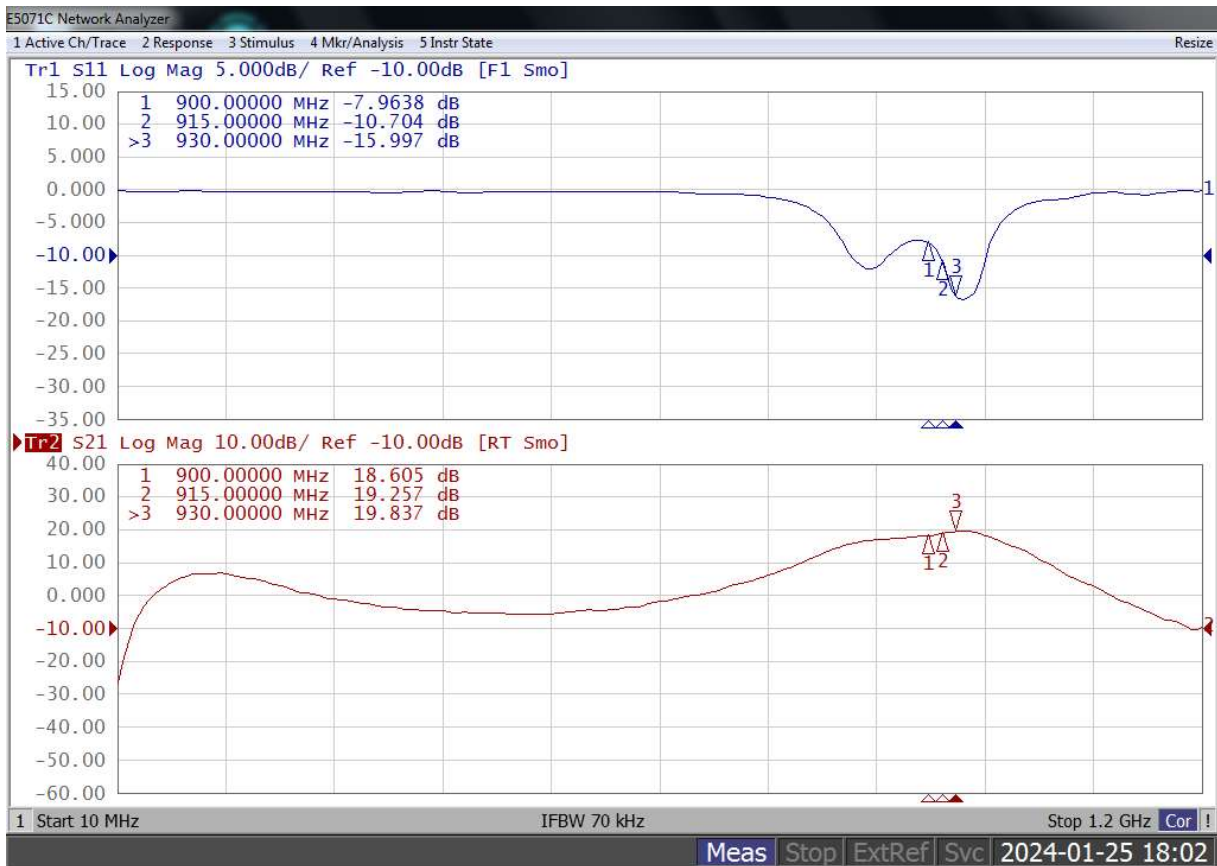




Designator	Footprint	Comment	Quantity
C1, C3	0603	47pF	2
C2, C4	1210	47pF	2
C5, C6, C7	1210	10 uF/100V	3
C8		2200 uF/63V	1
C9	0603	12 pF	1
C10	1210	8.2 pF	1
R1, R2, R3	0603	10 $\Omega$	3

## TYPICAL CHARACTERISTICS

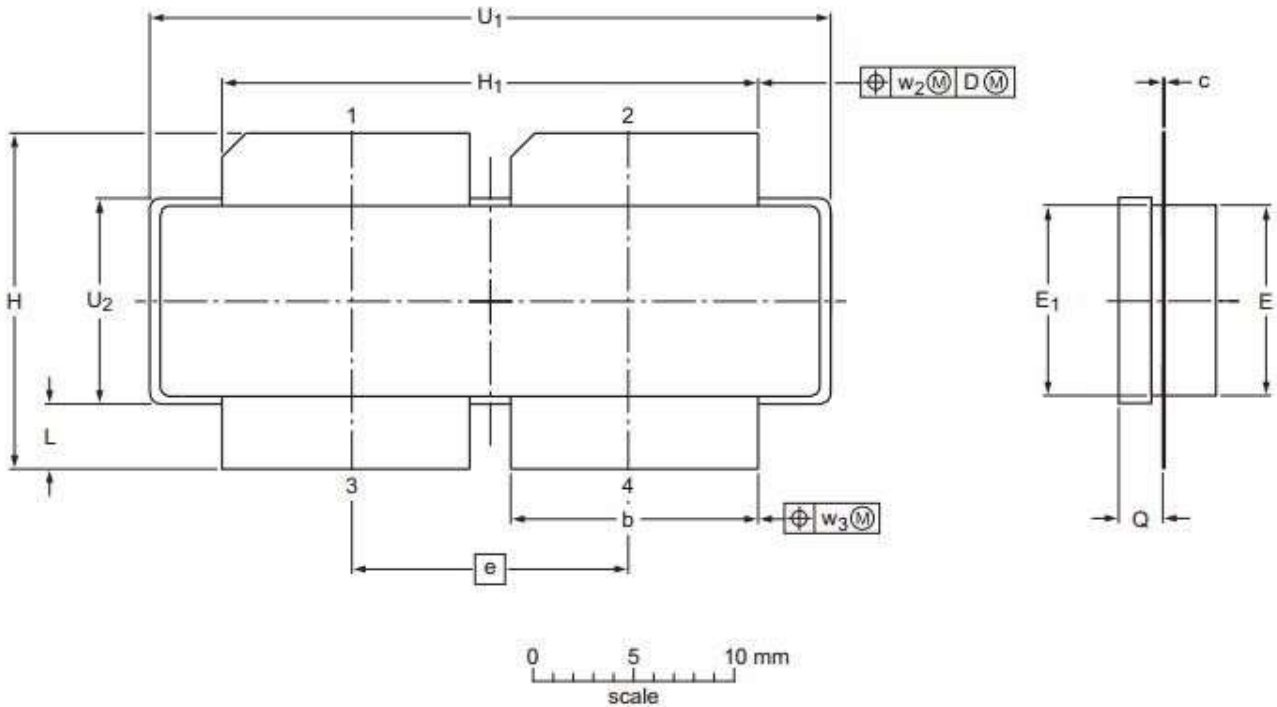
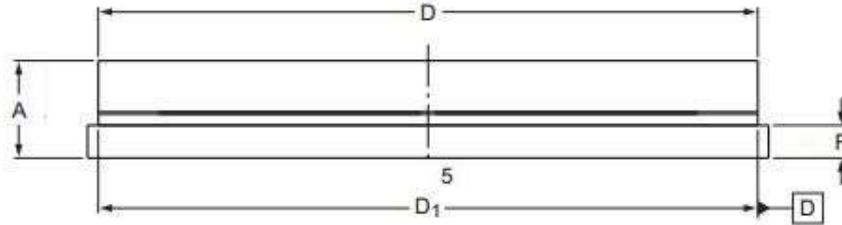
Figure 2: S11/S21 output from Network analyser (VDS= 50V, IDQ=500 mA Vgs =-3.3V)





### Package Outline

Earless flanged ceramic package; 4 leads (1、2—DRAIN、3、4—GATE、5—SOURCE)



UNIT	A	b	c	D	D <sub>1</sub>	e	E	E <sub>1</sub>	F	H	H <sub>1</sub>	L	Q	U <sub>1</sub>	U <sub>2</sub>	W <sub>2</sub>	W <sub>2</sub>
mm	4.7	11.81	0.18	31.55	31.52	13.72	9.50	9.53	1.75	17.12	25.53	3.48	2.26	32.39	10.29	0.25	0.25
	4.2	11.56	0.10	30.94	30.96		9.30	9.27	1.50	16.10	25.27	2.97	2.01	32.13	10.03		
inches	0.185	0.465	0.007	1.242	1.241	0.540	0.374	0.375	0.069	0.674	1.005	0.137	0.089	1.275	0.405	0.01	0.01
	0.165	0.455	0.004	1.218	1.219		0.366	0.365	0.059	0.634	0.995	0.117	0.079	1.265	0.395		

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4					03/12/2013



## Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2024/1/26	Rev 1.0	Preliminary datasheet creation

Application data based on: LSM-24-03

## Notice

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