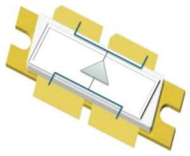
GaN 50V, 1200W, 915MHz RF Power Transistor

STBV101K5RD4



Single-Ended

Description

The STBV101K5RD4 is a 1200W CW capable, single ended, internally matched GaN HEMT, ideal for ISM or RF energy applications at 915MHz

There is no guarantee of performance when this part is used outside of stated frequencies.

Please notice that both leads at input and output side are internally connected, to configure this device as single ended ,shown as right picture.

- Typical RF performance at 915MHz applications

Vds=50V, Vgs=-4.2V, CW, Tc=25 degree C

Cooling	Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
Air/Water	915	59.95	989	74	18.7	60.97	1250	80

Recommended driver: ITGV20040J2 (50V LDMOS)

Applications

- 915MHz RF Energy
- P band power amplifier
- Avionics Power Amplifier

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically –5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically –5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum gate current	Igs	198	mA
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA T_C= 25°C, at Pd=350W	$R_{\theta JC}$	0.3	°C /W

Table 3. Electrical Characteristics (TA = 25℃ unless otherwise noted)

DC Characteristics (measured on wafer prior to packaging)

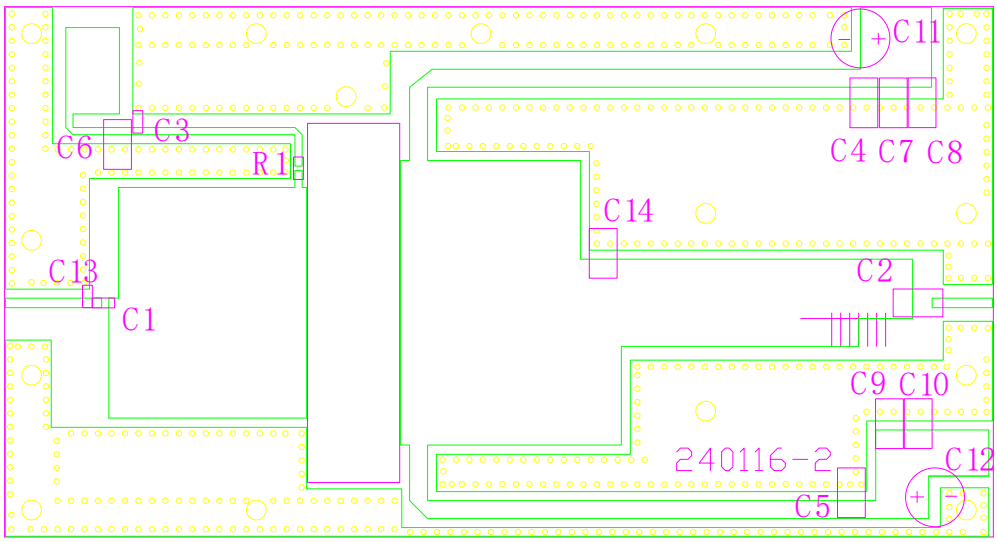
Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=198mA	V_{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID =198mA	$V_{GS(th)}$	-4	-	-2	V
Gate Quiescent Voltage	VDS =50V, IDS=500mA, Measured in Functional Test	$V_{GS(Q)}$		--3.3		V

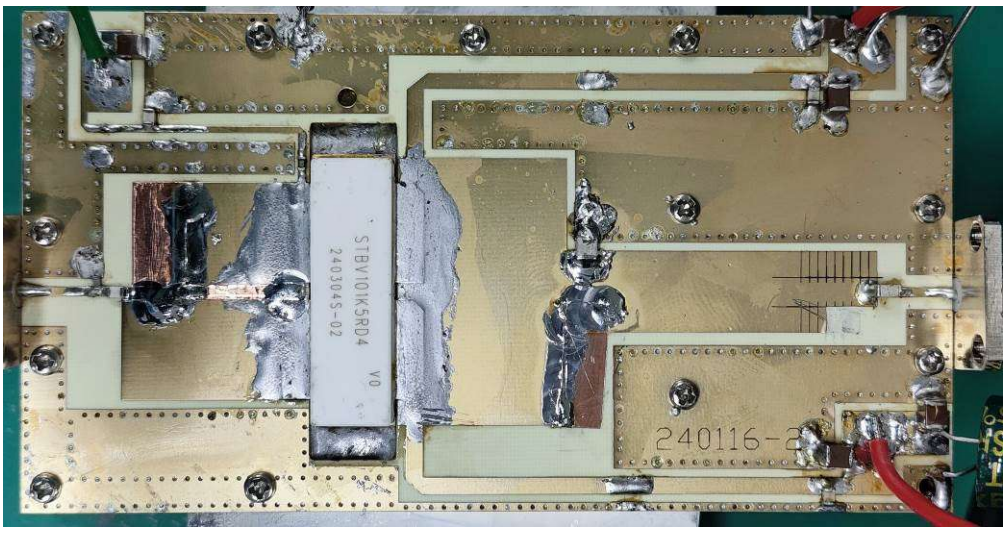
Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	915MHz, Pout=1200W pulse CW All phase, No device damages	VSWR		10:1		

Reference Circuit of Test Fixture Assembly Diagram

DXF file upon request

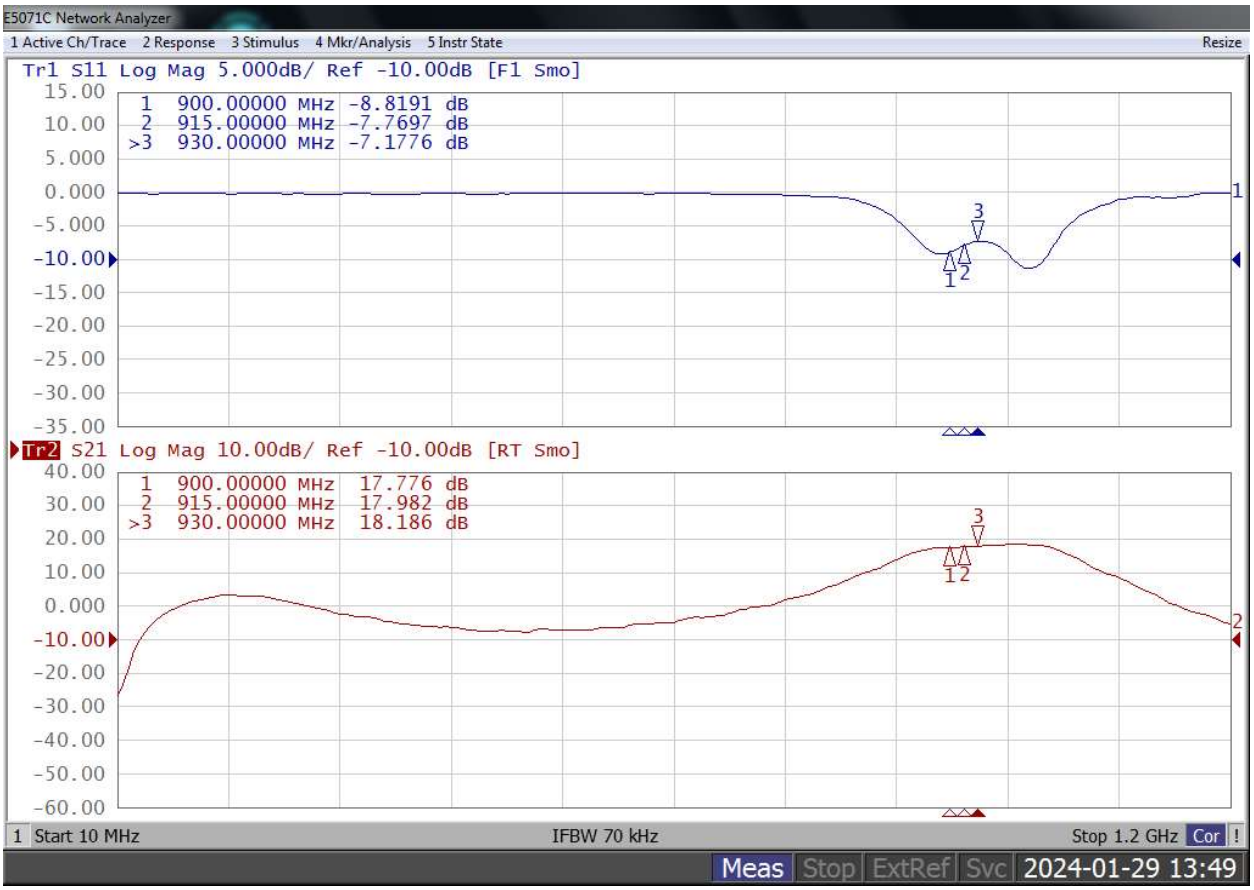




Designator	Footprint	Comment	Quantity
C1, C3	0603/0805	47pF	2
C2, C4, C5	1210	47pF	3
C6, C7, C8, C9, C10	1210	10uF/100V	5
C11, C12		2200uF/63V	2
C13	0603	12 pF	1
C14	1210	8.2 pF	1
R1	0603	10 Ω	1

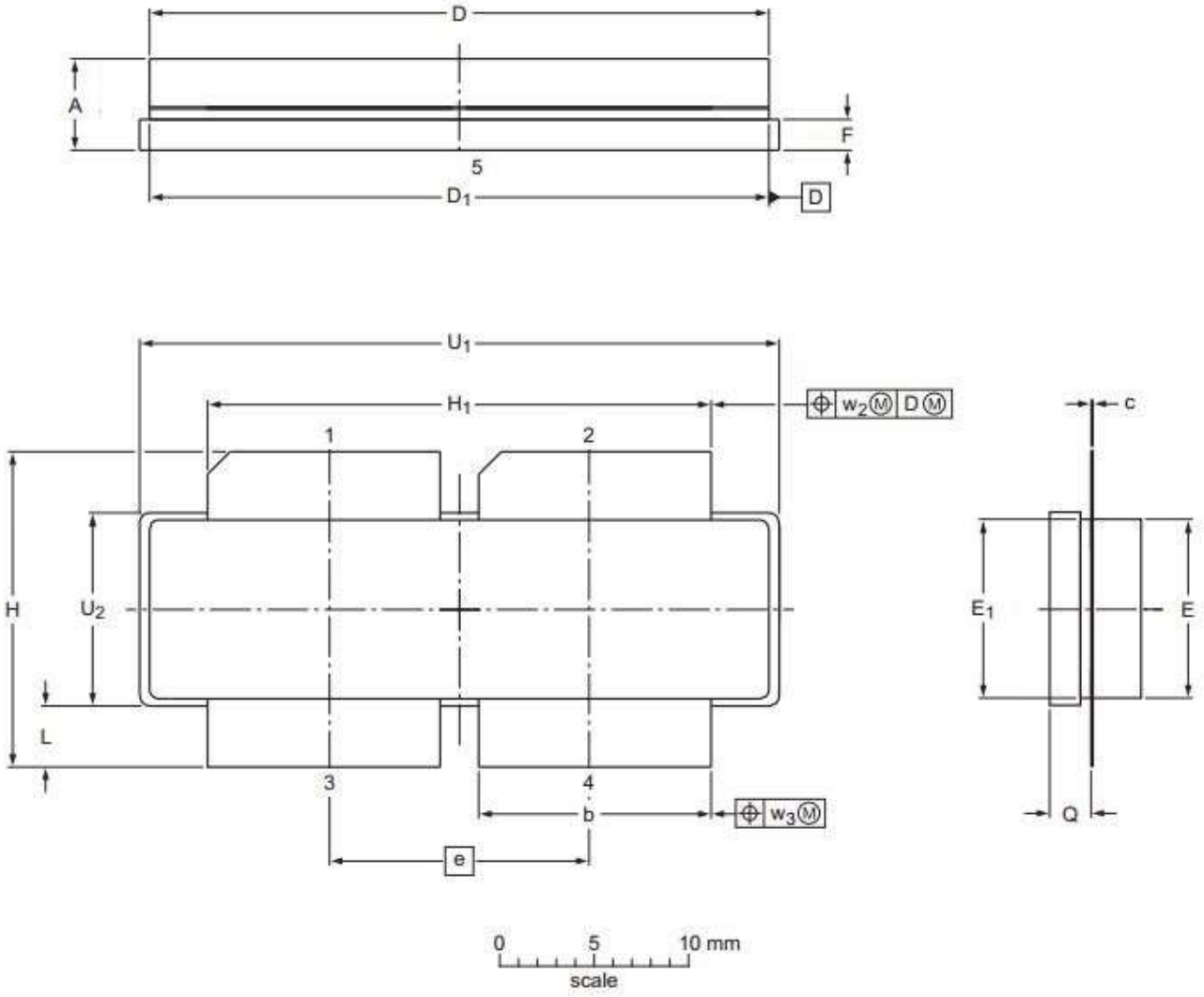
TYPICAL CHARACTERISTICS

Figure 2: S11/S21 output from Network analyser (VDS= 50V, IDQ=500 mA Vgs =-3.3V)



Package Outline

Earless flanged ceramic package; 4 leads（1、2—DRAIN、3、4—GATE、5—SOURCE）



UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	Q	U_1	U_2	W_2	W_2
mm	4.7 4.2	11.81 11.56	0.18 0.10	31.55 30.94	31.52 30.96	13.72	9.50 9.30	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.48 2.97	2.26 2.01	32.39 32.13	10.29 10.03	0.25	0.25
inches	0.185 0.165	0.465 0.455	0.007 0.004	1.242 1.218	1.241 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.137 0.117	0.089 0.079	1.275 1.265	0.405 0.395	0.01	0.01

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4					03/12/2013

Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2024/1/29	**Rev 1.0**	**Preliminary datasheet creation**

Application data based on: LSM-24-05

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