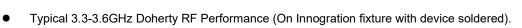
Innogration (Suzhou) Co., Ltd.

60W,28V Plastic RF LDMOS Transistor

Description

The ITEH36060C6 is a dual path 60-watt, highly rugged, LDMOS transistor, designed for driver applications at frequencies from 3.3 to 3.6GHz, in 10*6mm QFN plastic package, supporting surface mounted on PCB through high density grounding vias.

It can be configured as highly compact symmetrical Doherty ,ideal for high efficiency and low cost, DPD friendly driver stage of macro RRU or final stage of small cell for 4G/5G application within 3.3-3.6GHz.



Frog	Pulse CW Signal			P _{avg} =40dBm WCDMA Signal		
Freq (MHz)	P1dB Gain (dB)	P3dB (W)	Eff@P3dB (%)	Gp (dB)	Eff(%)	ACPR _{5M} (dBc)
3300	13.21	68.50	43.94	14.14	27.5	-32.44
3450	12.96	63.90	43.36	13.98	27	-34.26
3600	12.67	61.41	44.17	13.41	27	-35.42

Vds=28V Idq_main=180mA, Vgs_peak=2.15V

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- S band power ampliifer
- All 4G/5G cellular application within 3.3 to 3.6GHz
- Small cell

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
DrainSource Voltage	V _{DSS}	+65	Vdc
GateSource Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	Vdd	+28	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	Tc	+150	°C
Operating Junction Temperature	T٦	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	Balo	0.4	0000
T_{C} = 85°C, T_{J} =200°C, DC test	Rejc	0.4	°C/W



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Table 3. ESD Protection Characteristics

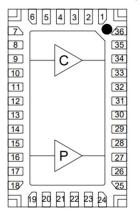
Test Methodology		Class				
Human Body Model (per JESD22A114)		Class 2				
Fable 4. Electrical Characteristics (TA = 25 $^{\circ}$ C unless otherwise)	e noted)					
Characteristic	Symbol	Min	Тур	Max	Unit	
OC Characteristics						
Drain-Source Voltage			05			
V _{GS} =0, I _{DS} =100uA	V _{(BR)DSS}		65		V	
Zero Gate Voltage Drain Leakage Current				4	μΑ	
$(V_{DS} = 28V, V_{GS} = 0 V)$	DSS			1		
GateSource Leakage Current				1	μA	
$(V_{GS} = 11 \text{ V}, V_{DS} = 0 \text{ V})$	GSS					
Gate Threshold Voltage	N		2		v	
$(V_{DS} = 28V, I_D = 600 \ \mu A)$	V _{GS} (th)					
Gate Quiescent Voltage			2.7		V	
$(V_{DD}$ = 28V, I _D = 100mA, Measured in Functional Test)	$V_{GS(Q)}$					
.oad Mismatch (In Innogration Test Fixture, 50 ohm system): $V_{ m c}$	_D = 28Vdc, I _{DQ} = ²	100 mA, f = 360	00 MHz			

VSWR 10:1 at 60W pulse CW Output Power

No Device Degradation

Figure 1: Pin Connection definition

Transparent top view (Backside grounding for source)



Pin No.	Symbol	Description
8,9,10,11	RF IN/Vgs1	RF Input, Vgs bias for main path
14,15,16,17	RF IN/Vgs2	RF Input, Vgs bias for peak path
32,33,34,35	RF OUT/VDD1	RF Output, VDD bias for Main path
26,27,28,29	RF OUT/VDD2	RF Output, VDD bias for Peak path
Rest pins	NC	No connection
2,5,7,12,13,18,20,23,25,30,31,36,	CND	DC/RF Ground. Must be soldered directly to heatsink or copper coin for
Package Base	GND	CW application.

3300-3600MHz application board

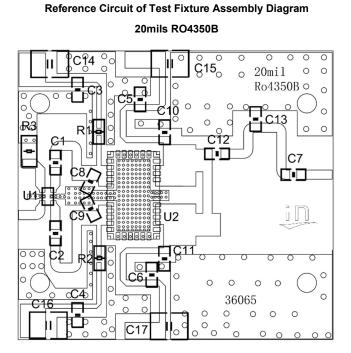


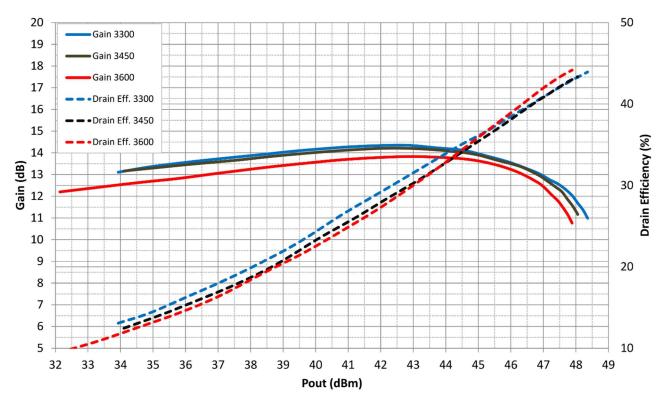
Figure 2. Test Circuit Component Layout

 Table 5. Test Circuit Component Designations and Values

Reference	Footprint	Value	Quantity
C1, C2, C3, C4, C5,	0603	8.2pF/250V	7
C6, C7	0003	8.2pr/230V	/
C8, C9	0603	1.6pF/250V	2
C10, C11	0603	0.9pF/250V	2
C12	0603	1.8pF/250V	1
C13	0603	0.5pF/250V	1
C14, C15, C16, C17	1210	10uF/100V	4
R1, R2	0603	10R	2
R3	0805	51R	1
U1	0805	C3337J5003AHF	1
U2	C6	ITEH36060C6 ^{vo}	1

TYPICAL CHARACTERISTICS

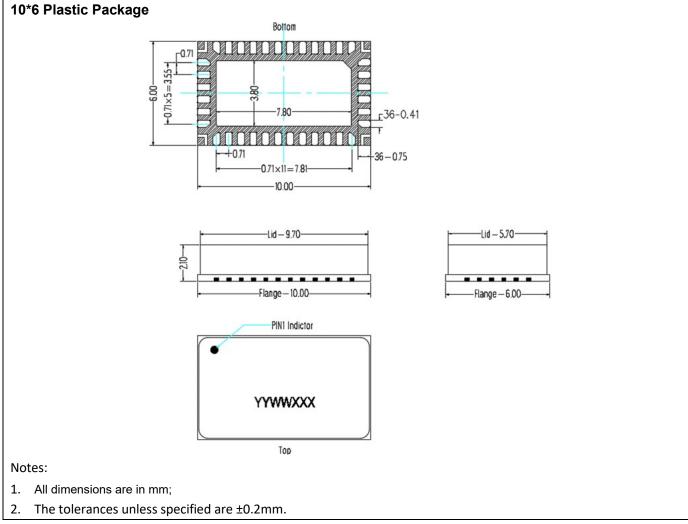
Figure 5. Power Gain and Drain Efficiency as function of Power Output at Idq=150mA







Package Dimensions



Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2023/1/5	Rev 1.0	Preliminary Datasheet

Application data based on ZBB-24-01

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