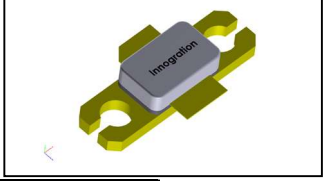
M2U1505V LDMOS TRANSISTOP

Document Number: M2U1505V
Preliminary Datasheet V1.0

1500MHz, 55W, 50V High Power RF LDMOS FETs

M2U1505V



Description

The M2U1505V is a 55-watt P1dB, highly rugged, unmatched LDMOS FET, designed for wide-band commercial and industrial applications at frequencies HF to 1.5 GHz.

It can support pulsed, CW or any modulated signal in form of linear or saturated operations.

•Typical Performance (On Innogration 2 kinds of narrow band fixtures with device soldered):

V_{ds}= 50V, V_{gs}=3V,I_{dq}=10mA						
Freq(MHz)	Test signal	P-1(dBm)	P-1Gain(dB)	P-3(dBm)	P-3(W)	Eff(%)
915	Pulsed	49.19	22.0	49.66	92.5	65
	CW	48.74	21.7	49.17	82.7	62
1030-1090	Pulsed	48.90	18.7	49.64	92.1	59

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- 2-30MHz (HF or Short wave communication)
- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 118 -140MHz (Avionics)
- L band (1200-1400MHz)
- 136-174MHz (Commercial ground communication)
- 160-230MHz (TV VHF III)
- 30-512MHz (Jammer, Ground/Air communication)
- 470-860MHz (TV UHF)
- 100kHz - 1000MHz (ISM, instrumentation)
- Avionics （960-1215MHz）

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	110	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test	RθJC	1.6	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0, I_{DS}=1.0mA	$V_{(BR)DSS}$		110		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS(th)}$	——	2.73	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 10 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3	——	V
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{ISS}		50		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{OSS}		20		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz)	C_{RSS}		0.6		pF
Functional Tests (In Demo Test Fixture, 50 ohm system) V_{DD} = 50 Vdc, I_{DQ} = 10mA, f = 915 MHz, CW Signal Measurements, Pin=26dBm					
Power Gain@Pout	G_p	——	22	——	dB
Output Power	Pout	55	60		W
Drain Efficiency@Pout	η_D	——	60	——	%
Input Return Loss	IRL	——	-5	——	dB

TYPICAL CHARACTERISTICS

Figure 1: Pulsed CW Gain and Power Efficiency as a Function of Pout at 915MHz

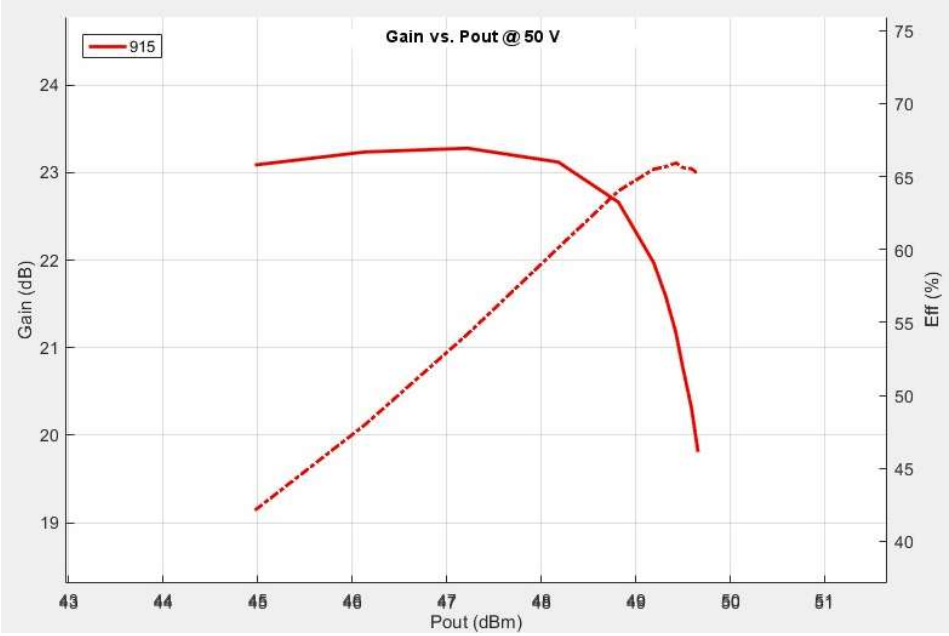


Figure 2: Network analyzer output S11/S21

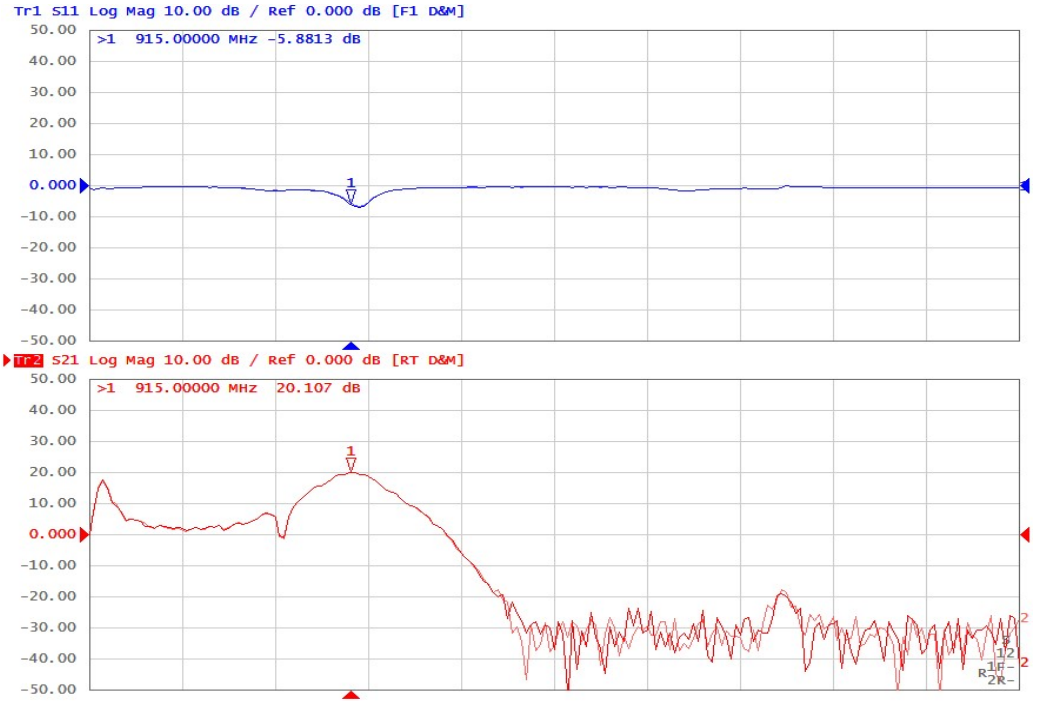
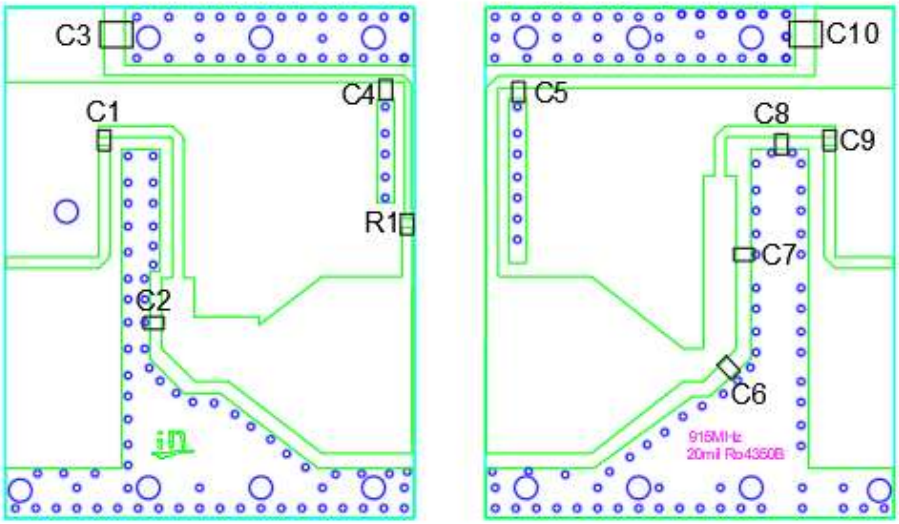


Figure 3. Test Circuit Component Layout

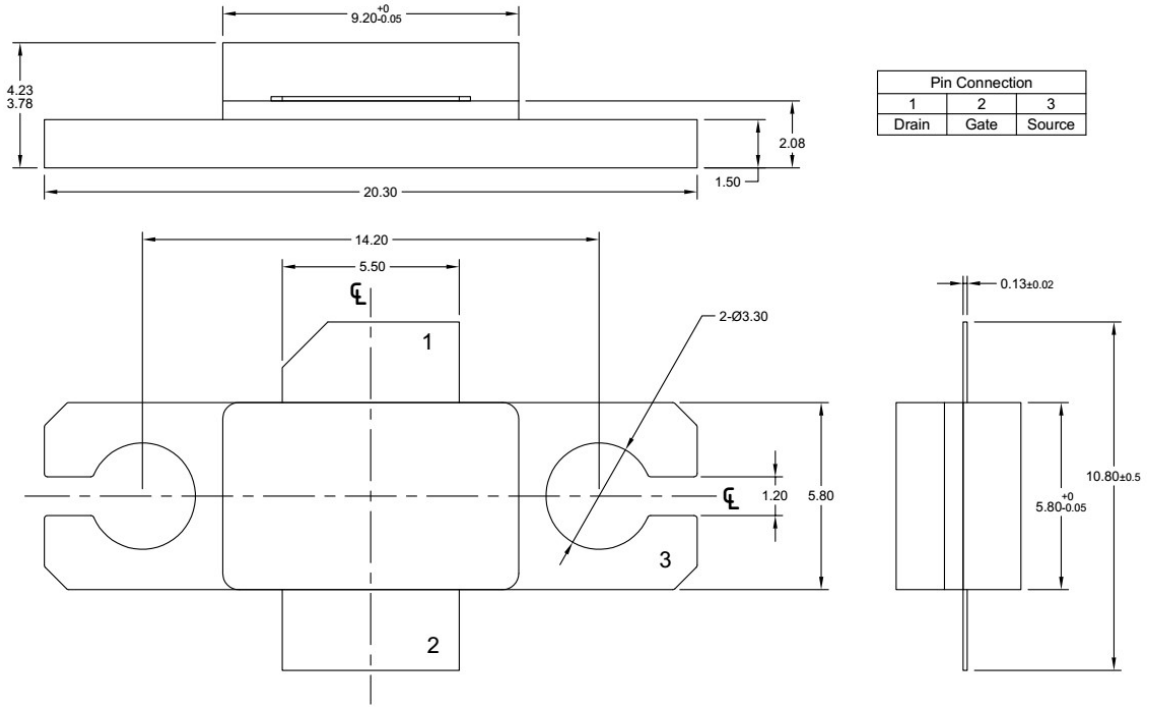
(PCB Roger 4350B 20Mil, PCB file upon request)



Component	Value	Description
C1,C4,C5,C9	22pF	ATC600S
C2,C6	12pF	ATC600S
C3,C10	10uF	TDK1206
C7	6.8pF	ATC600S
C8	3.0pF	ATC600S
C8	1.5pF	ATC600S
R1	10 Ω	--

Package Outline

Flanged ceramic package; 2 leads



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-GXB					10/10/2017

Figure 1. Package Outline PKG-G2E

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2024/2/23	**V1.0**	**Preliminary Datasheet Creation**

Application data based on HJ-24-02/03

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