GaN HEMT 50V, 700W, 3.7-4.0GHz Full band RF Power Transistor

STCV40700CY4V

Description

The STCV40700CY4V is a 700-watt, internally matched GaN HEMT, designed for 5G cellular applications with frequencies from 3.7-4.0GHz, **enabled by wide band VBW capability to support IBW typically 200MHz.**.

It can be configured as asymmetrical Doherty for 5G application, delivering 90W average power, according to normal 9dB back off.

There is no guarantee of performance when this part is used in applications designed Outside of these frequencies.

- Typical Doherty Pulsed CW and 1C W--CDMA Characterization Performance:

V_{DD} = 50 Vdc, I_{DQA} =280 mA, V_{GSB} = –5.8Vdc,1C WCDMA; Signal PAR = 10 dB @ 0.01% Probability on CCDF.

Freq (GHz)	Pulse CW Signal(1)			P_{avg}=49.5dBm WCDMA Signal(2)		
	GainP1 (dB)	P3 (dBm)	P3 (W)	Gp (dB)	η_D (%)	$ACPR_{5M}$ (dBc)
3.7	9.97	58.55	716	9.99	41.04	-28.95
3.8	10.31	58.97	789	10.74	43.46	-34.99
3.9	10.30	58.97	789	10.90	40.88	-34.58
4.0	10.80	58.53	712	10.90	39.39	-31.55

Recommended driver：STBV42130C9(1 stage Doherty discrete) or SMBV3740-201（2 stages Doherty MCM）

Applications

- Asymmetrical Doherty amplifier within N78 5G band
- S band power amplifier

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

Turning the device ON

1. Set VGS to the pinch—off (VP) voltage, typically –5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically –5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Figure 1: Pin Connection definition

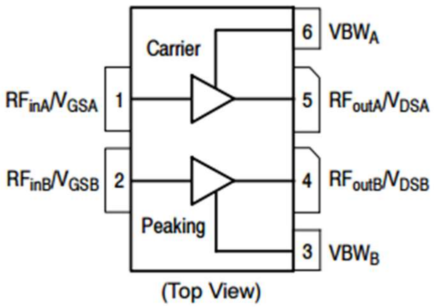


Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain—Source Voltage	V_{DSS}	+200	Vdc
Gate—Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum gate current	Igs	116	mA
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA T_C= 85°C, Pout=90W, 3.7GHz Doherty application board	$R_{\theta JC}$	0.7	°C /W

Table 3. Electrical Characteristics (TA = 25℃ unless otherwise noted)

DC Characteristics (main path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=40mA	V_{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 40mA	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	VDS =50V, IDS=300mA, Measured in Functional Test	$V_{GS(Q)}$		-3.3		V

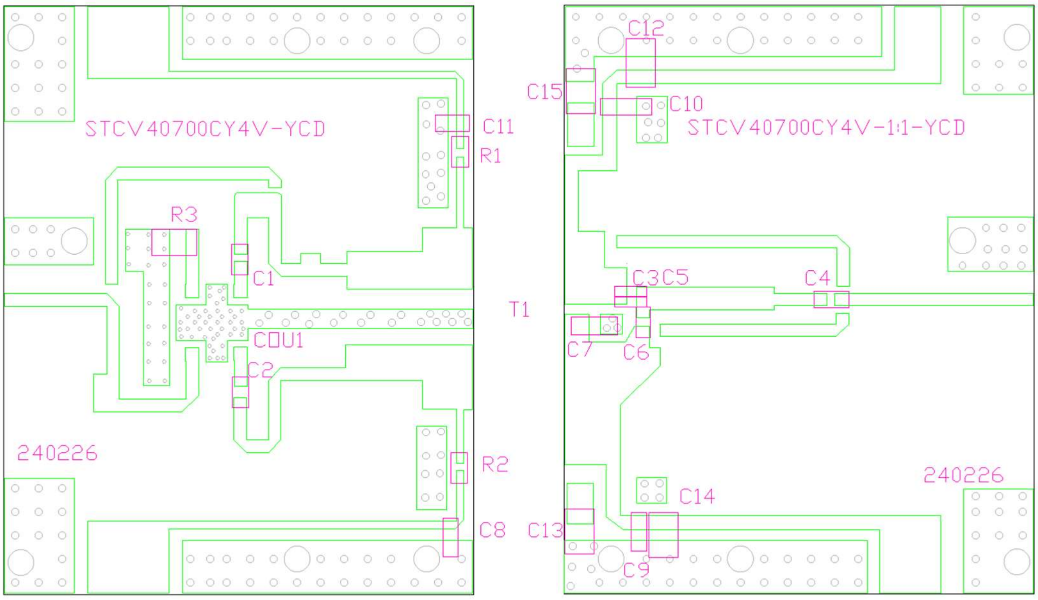
DC Characteristics (peak path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=60mA	V_{DSS}		200		V
Gate Threshold Voltage	VDS =10V, ID = 60mA	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	VDS =50V, IDS=450mA Measured in Functional Test	$V_{GS(Q)}$		-3.3		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	3.7GHz, Pout=90W WCDMA 1 Carrier in Doherty circuit All phase, No device damages	VSWR		10:1		

Figure 3: Picture of application board Doherty circuit for 3.7-4.0GHz



Part	Quantity	Description	Part Number	Manufacture
C1,C2,C4 C11,C8,C9,C10	7	8.2pFHigh Q Capacitor	251SHS8R2BSE	TEMEX
C3,C5	2	0.7pFHigh Q Capacitor	251SHS0R7BSE	TEMEX
C6	1	1.2pFHigh Q Capacitor	251SHS1R2BSE	TEMEX
C7	1	0.5pFHigh Q Capacitor	251SHS0R5BSE	TEMEX
C12,C13,C14,C15	4	10uF MLCC	RS80R2A106M	MARUWA
R1,R2	2	10Ω Power Resistor	ESR03EZPF100	ROHM
R3	1	51Ω Power Resistor	RFR50-20CT0421B	YT
COUT1	1	3 dB Bridge	XC3500P-03S	ANAREN
T1	1	700W GaN Dual Transistor	STCV404700CY4V	Innogration

Figure 4: Efficiency and power gain as function of Pout

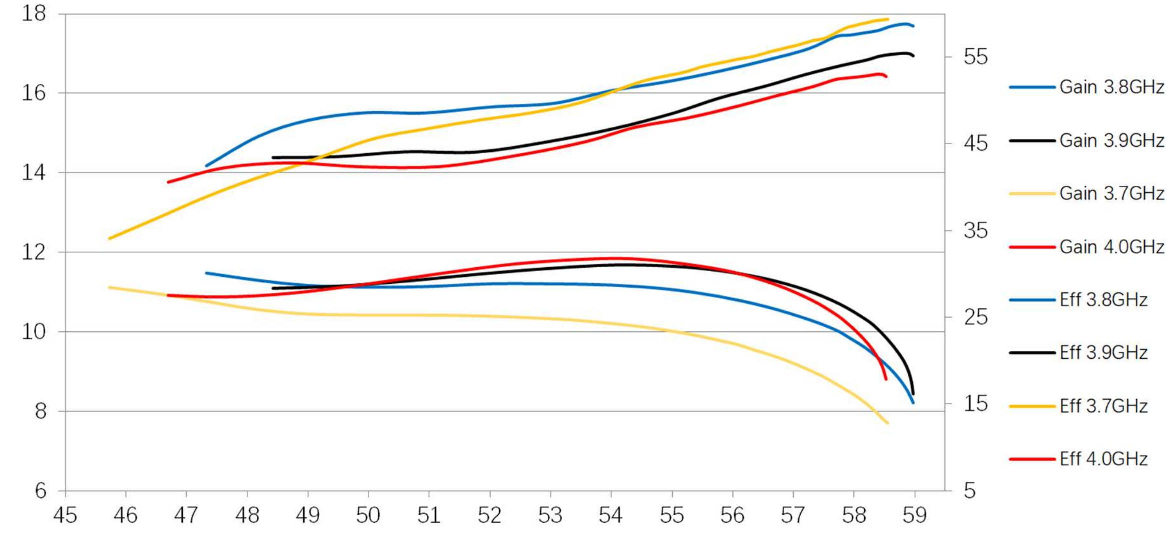
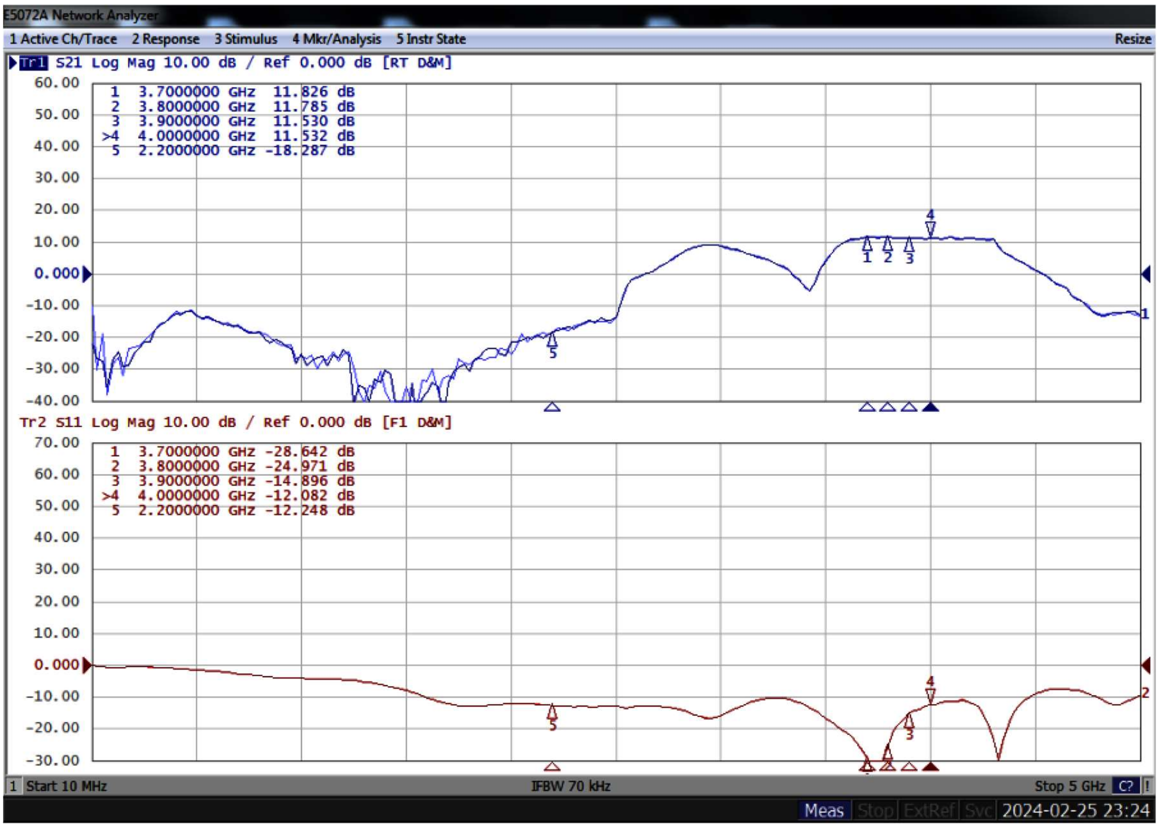
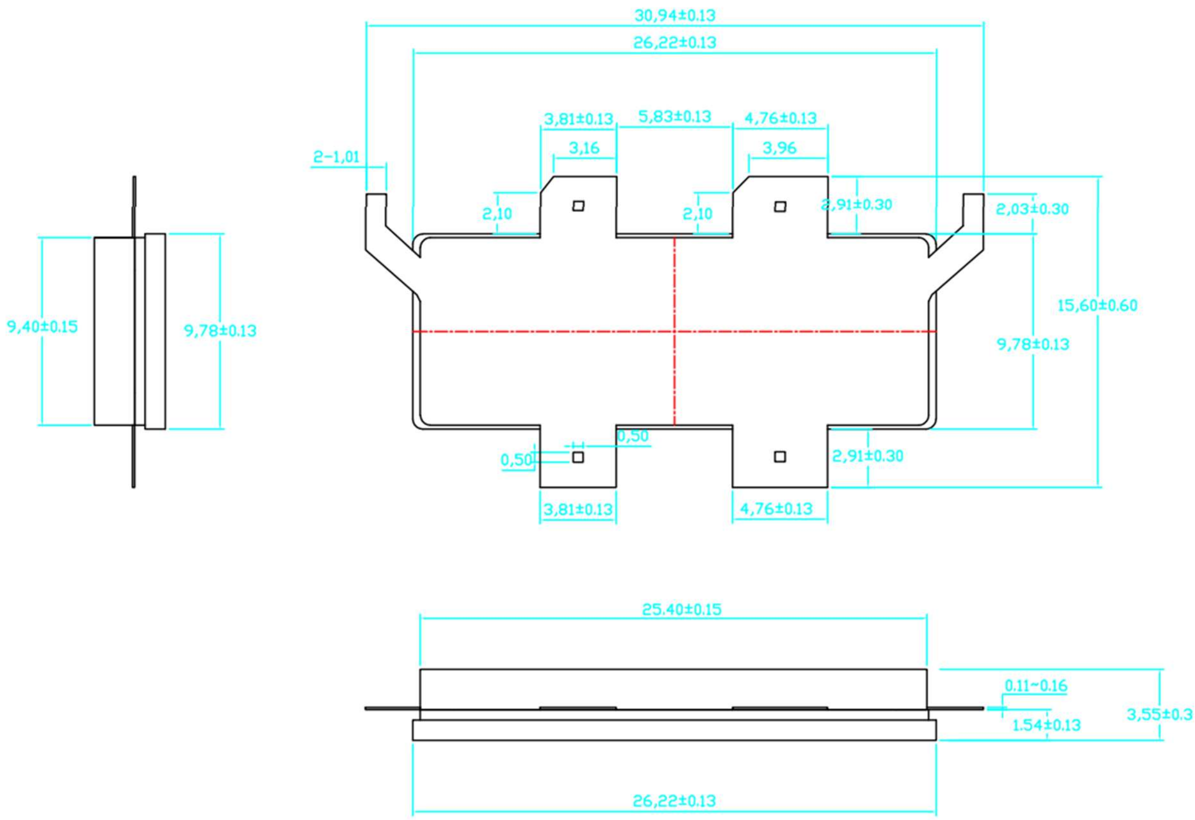


Figure 5: Network analyzer output, S11 and S21



Earless Flanged Ceramic Package; 6 leads- CY4V



Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2024/2/26	V1.0	Preliminary Datasheet Creation

Application data based on LWH-24-09

Notice

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