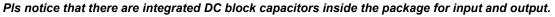
Innogration (Suzhou) Co., Ltd.

GaN HEMT 50V, 15W*2, 4.4-5GHz Fully matched transistor

Description

The SMAV50030C6 is a dual path 15W*2,fully matched transistor, operating from 4.4-5GHz.Each 15W path is independent and identical which enables great flexibilities of multiple amplifier configurations (see below) It features high gain, high efficiency, wide band and low cost, in 10*6mm open cavity plastic package. In particularly it helps size limited amplifier design, easy to use, thanks to its 500hm in and out configuration. There is no guarantee of performance when this part is used outside of stated frequencies.



Typical pulsed CW performance Characterization Performance of half section

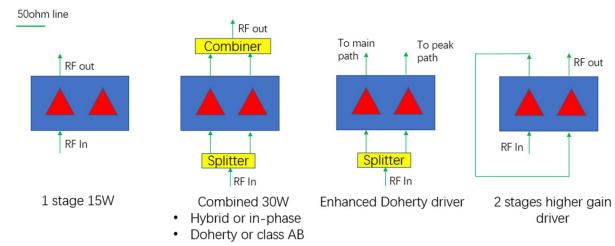
VDD = 50 Vdc, IDQ = 20mA, VGs= –3Vdc, pulsed width 20us and 10% duty cycle

Freq(MHz)	P-1(dBm)	P-1Gain(dB)	P-3(dBm)	P-3(W)	EFF (%)
4400	40.38	17.8	42.33	17.1	51.7
4600	40.48	16.8	42.32	17.1	51.2
4800	40.61	16.2	42.31	17.0	54.8
5000	40.56	15.4	42.19	16.5	58.7

Applications

- Sub-5GHz power amplifier
- Driver stage for 5G power amplifier within N79, like 4.4-4.6, 4.8-5GHz
- C band pulsed power amplifier like 4.4-5GHz

Typical configuration



Hybrid Splitter and combiner recommendation: Yantel HC55703 (2*1.25mm IL<0.35dB, 4W CW capabable)

SMAV50030C6



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Important Note: Proper Biasing Sequence for GaN HEMT Transistors

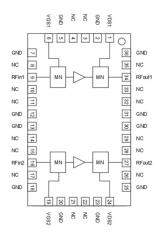
Turning the device ON

- 1. Set VGS to the pinch--off (VP) voltage, typically -5 V
- 2. Turn on VDS to nominal supply voltage
- 3. Increase VGS until IDS current is attained
- 4. Apply RF input power to desired level

Turning the device OFF

- 1. Turn RF power off
- 2. Reduce VGS down to VP, typically -5 V
- 3. Reduce VDS down to 0 V
- 4. Turn off VGS

Figure 1: Pin Connection definition--- transparent top view (Backside grounding for source)



Pin No.	Symbol	Description	
6	Vgs1	Vgs bias for path 1	
1	VDD1	Vdd bias for path 1	
9	RFIN1	RF Input for path 1	
34	RFOUT1	RF Output for path 1	
19	Vgs2	Vgs bias for path 2	
24	VDD2	Vdd bias for path 2	
16	RFIN2	RF Input for path 2	
27	RFOUT2	RF Output for path 2	
Rest pins	NC	No connection	
Package Base	GND	DC/RF Ground.	

Table 1. Maximum Ratings (half section)

Rating	Symbol	Value	Unit
DrainSource Voltage	V _{DSS}	+200	Vdc
GateSource Voltage	V _{GS}	-8 to +0.5	Vdc
Operating Voltage	V _{DD}	55	Vdc
Maximum gate current	lgs	2	mA
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	Tc	+150	°C
Operating Junction Temperature	TJ	+225	°C

Table 2. Thermal Characteristics (half section)

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA	Date	10	
T _c = 85°C, 4.6GHz Pout=16W pulsed CW	Rejc	10	°C /W

(1) The thermal resistance is acquired by FEA model, which was calibrated by IR measurement, the value shall be applied to reliability.

(2) The reference Tcase temperature 85° C is apply on the backside of package.

(3) The device on application board is soldered onto the 20mil Rogers PCB with $108 \times \Phi 0.25$ mm via hole beneath the package backside.

Table 3. Electrical Characteristics (TA = 25℃ unless otherwise noted)

DC Characteristics (half section, measured on wafer prior to packaging)

Characteristic	Conditions		Min	Тур	Max	Unit
Drain-Source Breakdown Voltage	-Source Breakdown Voltage VGS=-8V; IDS=2mA			200		V
Gate Threshold Voltage	VDS =10V, ID = 2mA	V _{GS(th)}	-4	-3.2	-2	V
Gate Quiescent Voltage	VDS =50V, IDS=20mA, Measured in Functional Test	V _{GS(Q)}		-3		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Тур	Max	Unit
Load mismatch capability	4.6G, Pout=42dBm Pulsed CW,					
	All phase,	VSWR		10:1		
	No device damages					

Figure 2: Figure 1: Efficiency and power gain as function of Pout

VDD = 50 Vdc, IDQ = 20 mA, Pulse width=20us, duty cycle=20%

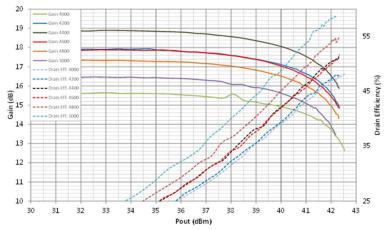


Figure 3: Application board layout info of half section (RO4350B 20mils)

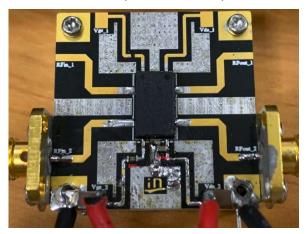


Figure 4: S11/S21 output from Network analyser of half section

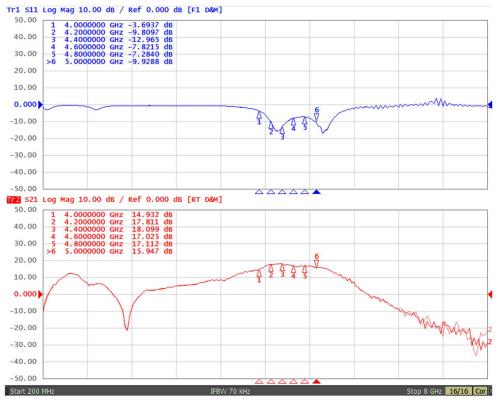
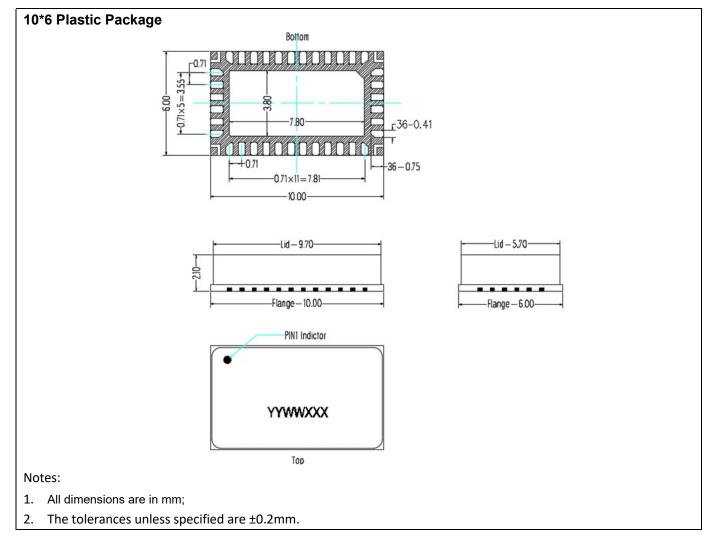


Table 4: 1 Carrier WCDMA back off performance of half section

P(dBm)	Freq(MHz)	4400	4600	4800	5000
28		-35.8	-39.1	-39.0	-41.7
29		-35.5	-38.8	-39.1	-41.4
30	ACPR(dBc)	-35.1	-38.4	-38.8	-41.2
31	ACFR(UDC)	-34.7	-38.0	-38.5	-40.6
32		-34.4	-37.4	-37.8	-39.6
33		-33.8	-36.6	-37.2	-38.3
28		18.3	17.5	16.9	16.1
29	Gain(dB)	18.3	17.4	16.9	16.0
30		18.3	17.4	16.8	16.0
31		18.2	17.3	16.8	16.0
32		18.1	17.3	16.7	15.9
33		18.0	17.1	16.6	15.8
28		12.9	12.7	13.6	14.7
29		14.5	14.3	15.4	16.6
30	Eff(%)	16.2	15.9	17.2	18.6
31		18.1	17.9	19.3	20.9
32		20.3	19.9	21.5	23.3
33		22.5	22.3	24.0	26.0

Package Dimensions



Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status	
2021/10/21	V1.0	Preliminary Datasheet Creation	
2021/11/19	V1.1	Add recommended splitter and combiner	
2022/10/8	V1.2	Modify the typo of pin definition	

Application data based on: HJ-21-15

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