



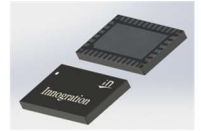
GaN HEMT 50V, 15W*2, 2.5-4.2GHz Fully matched transistor

Description

The SMAV42030C6 is a dual path 15W*2, fully matched transistor, operating from 2.5-4.2GHz. Each 15W path is independent and identical which enables great flexibilities of multiple amplifier configurations (see below) It features high gain, high efficiency, wide band and low cost, in 10*6mm open cavity plastic package. In particular it helps size limited amplifier design, easy to use, thanks to its 50ohm in and out configuration. There is no guarantee of performance when this part is used outside of stated frequencies.

Pls notice that there are integrated DC block capacitors inside the package for input and output. No additional external capacitor needed.

SMAV42030C



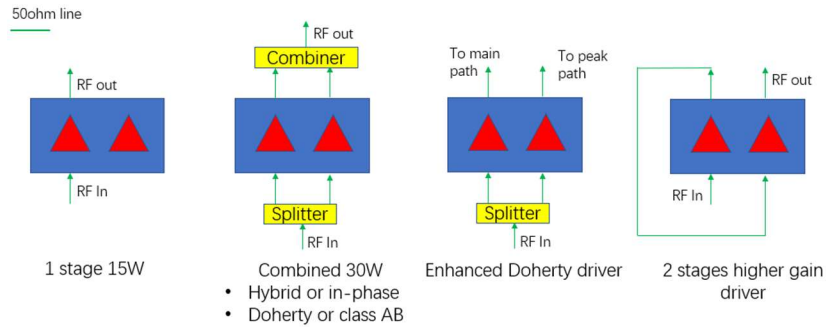
- Typical pulsed CW performance Characterization Performance of **half section**

VDS= 50V, VGS=-3.04V, Idq=20mA					
Pulse Peak Power					
Freq(MHz)	P-1(dBm)	P-1Gain (dB)	P-3(dBm)	P-3(W)	Eff (%)
2500	40.79	14.0	42.54	17.9	51.4
2600	41.45	14.0	42.74	18.8	55.3
2700	41.49	13.8	42.77	18.9	55.8
2800	41.69	13.2	42.86	19.3	58.0
2900	41.70	13.9	42.76	18.9	58.7
3000	41.42	14.3	42.58	18.1	57.0
3100	41.38	13.8	42.58	18.1	56.9
3200	41.36	13.1	42.38	17.3	55.3
3300	41.33	13.0	42.21	16.6	55.5
3400	41.35	13.6	42.09	16.2	55.4
3500	41.18	14.1	41.98	15.8	55.6
3600	40.93	13.9	41.86	15.3	53.6
3700	40.87	13.4	41.95	15.7	53.1
3800	40.64	13.5	42.02	15.9	53.0
3900	40.65	13.6	41.95	15.7	53.1
4000	40.24	14.0	41.82	15.2	54.9

● Applications

- Sub-5GHz power amplifier
- Driver stage for 5G power amplifier within 2.5-4.2GHz, covering N41, N77, N78
- S band pulsed power amplifier like 2.7-3.5GHz

Typical configuration



Hybrid Splitter and combiner recommendation for major sub bands

Yantel HC35T03 (2*1.25mm IL<0.3dB 4W) for 3.3-3.8GHz and HC25T03 (2*1.25mm IL<0.3dB 4W) for 2.5-2.7GHz

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

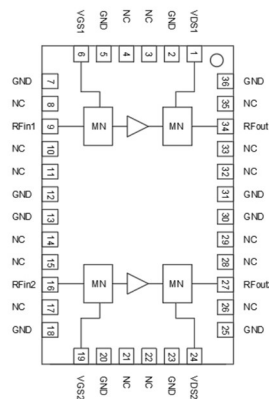
Turning the device ON

1. Set VGS to the pinch-off (VP) voltage, typically -5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically -5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Figure 1: Pin Connection definition--- transparent top view (Backside grounding for source)



Pin No.	Symbol	Description
6	Vgs1	Vgs bias for path 1
1	VDD1	Vdd bias for path 1
9	RFIN1	RF Input for path 1
34	RFOUT1	RF Output for path 1
19	Vgs2	Vgs bias for path 2
24	VDD2	Vdd bias for path 2
16	RFIN2	RF Input for path 2
27	RFOUT2	RF Output for path 2
Rest pins	NC	No connection
Package Base	GND	DC/RF Ground.



Table 1. Maximum Ratings (half section)

Rating	Symbol	Value	Unit
Drain—Source Voltage	V_{DSS}	+200	Vdc
Gate—Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum gate current	I_{gs}	2	mA
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics (half section)

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA $T_c = 85^\circ\text{C}$, 3.6GHz Pout=16W pulsed CW	$R_{\theta JC}$	10	°C /W

- (1) The thermal resistance is acquired by FEA model, which was calibrated by IR measurement, the value shall be applied to reliability.
- (2) The reference T_{case} temperature 85°C is apply on the backside of package.
- (3) The device on application board is soldered onto the 20mil Rogers PCB with $108 \times \Phi 0.25\text{mm}$ via hole beneath the package backside.

Table 3. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

DC Characteristics (half section, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = -8\text{V}$; $I_{DS} = 2\text{mA}$	V_{DSS}		200		V
Gate Threshold Voltage	$V_{DS} = 10\text{V}$, $I_D = 2\text{mA}$	$V_{GS(th)}$	-4	-3.2	-2	V
Gate Quiescent Voltage	$V_{DS} = 50\text{V}$, $I_{DS} = 20\text{mA}$, Measured in Functional Test	$V_{GS(Q)}$		-3		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	3.6G, Pout=42dBm Pulsed CW, All phase, No device damages	VSWR		10:1		

Figure 2: Efficiency and power gain as function of Pout ($V_{DD} = 50\text{Vdc}$, $I_{DQ} = 20\text{mA}$, Pulse width=50us, duty cycle=20%)

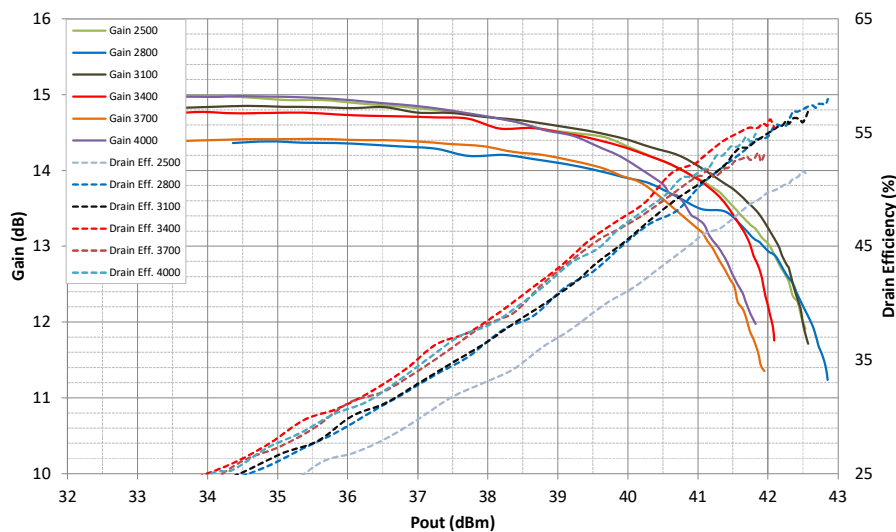


Figure 3: Application board layout info (RO4350B 20mils)

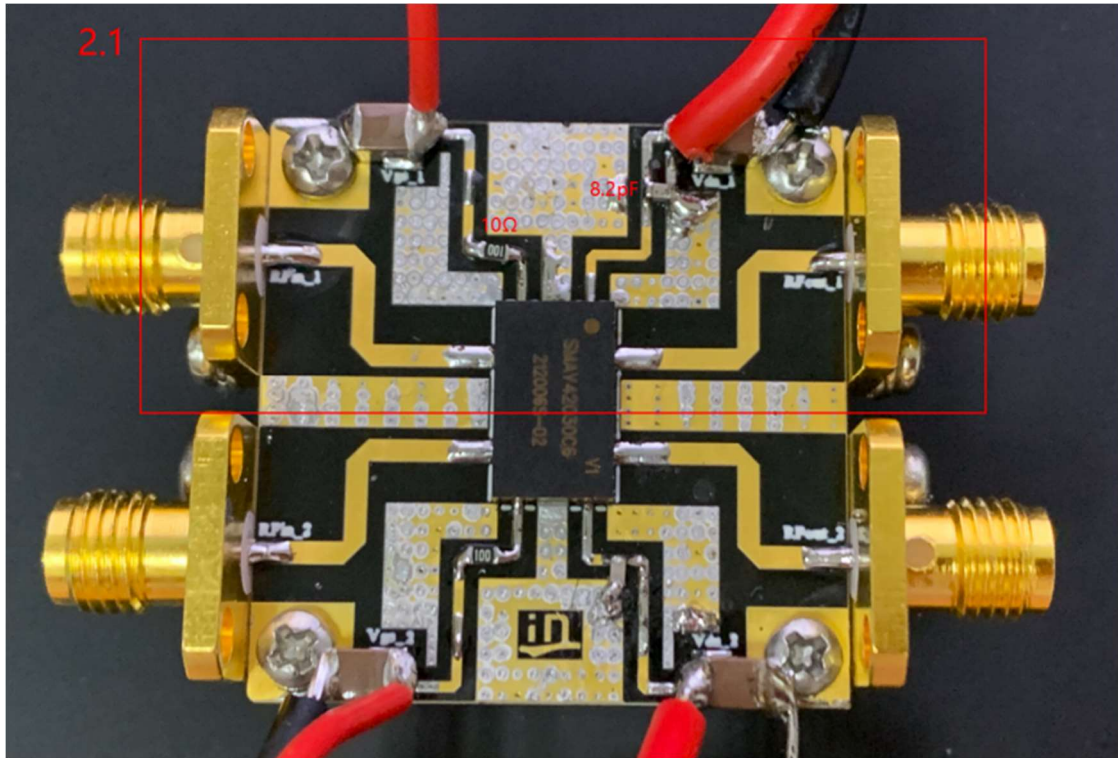
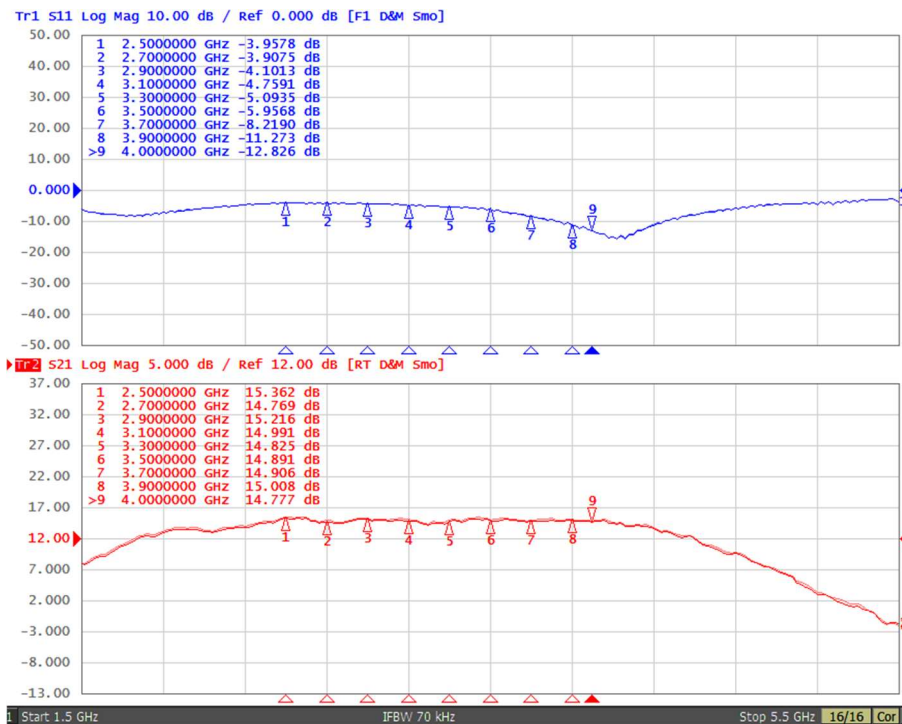


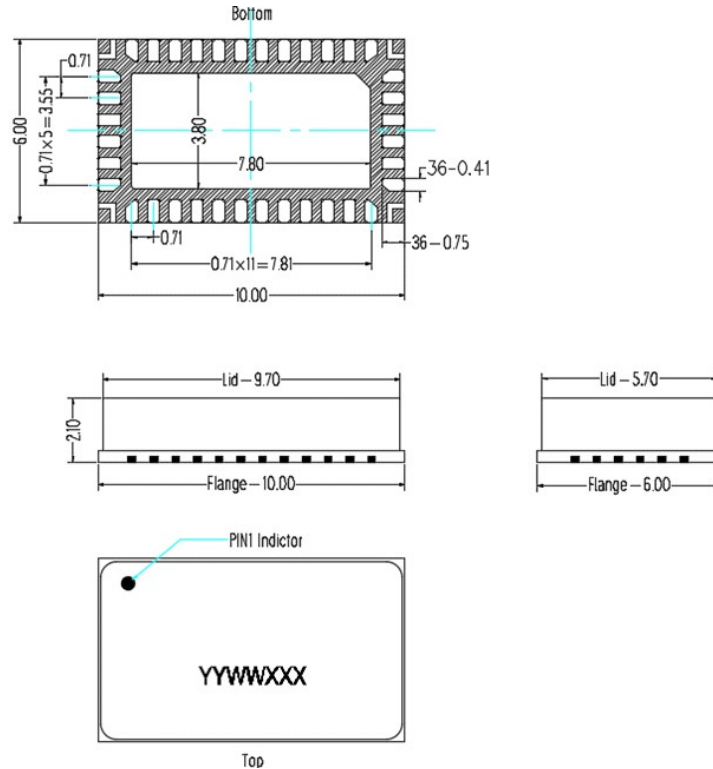
Figure 4: S11/S21 output from Network analyser of half section





Package Dimensions

10*6 Plastic Package



Notes:

1. All dimensions are in mm;
2. The tolerances unless specified are ±0.2mm.

Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2020/12/18	V1.0	Preliminary Datasheet Creation
2021/5/13	V1.1	Preliminary Datasheet Creation
2021/11/19	V1.2	Add recommended hybrid splitter and combiner
2022/10/8	V1.3	Modify the typo of pin definition and demo board picture

Application data based on: HJ-21-04

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