

MC0530RS LDMOS TRANSISTOR

Document Number: MC0530RS
Product Datasheet V1.0

300W, P band High Power RF LDMOS FETs

MC0530RS

Description

The MC0530RS is a 300-watt, unmatched, high ruggedness, single ended LDMOS FETs, designed for P band application up to 0.7GHz.

It can be used in Class AB/B and Class C for any pulse and CW signal.

- Typical CW Performance (On Innogration fixture with device soldered):

$V_{ds} = 28V, I_{dq} = 100mA, V_{gs} = 2.76V$

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff (%)	P1dB Gain (dB)	P3dB (dBm)	P3dB (W)	P3dB Eff (%)
500	54.25	266.32	62.95	17.7	54.99	315.19	69



Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- P band pulse or CW amplifier
- ISM applications

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+95	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+36	Vdc
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_c	+150	°C
Operating Junction Temperature	T_j	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_c = 85^\circ C, T_j = 200^\circ C, DC \text{ test}$	$R_{\theta JC}$	0.2	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics ($T_A = 25^\circ C$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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DC Characteristics

Zero Gate Voltage Drain Leakage Current ($V_{DS} = 95V, V_{GS} = 0V$)	I_{DSS}			100	μA
Zero Gate Voltage Drain Leakage Current ($V_{DS} = 28V, V_{GS} = 0V$)	I_{DSS}			1	μA
Gate--Source Leakage Current ($V_{GS} = 10V, V_{DS} = 0V$)	I_{GSS}			1	μA

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Gate Threshold Voltage ($V_{DS} = 28V, I_D = 450 \mu A$)	$V_{GS(th)}$	1.9	V
Gate Quiescent Voltage ($V_{DD} = 28V, I_D = 100mA$, Measured in Functional Test)	$V_{GS(Q)}$	2.76	V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): $V_{DD} = 28Vdc, I_{DQ} = 100mA, f = 700MHz$

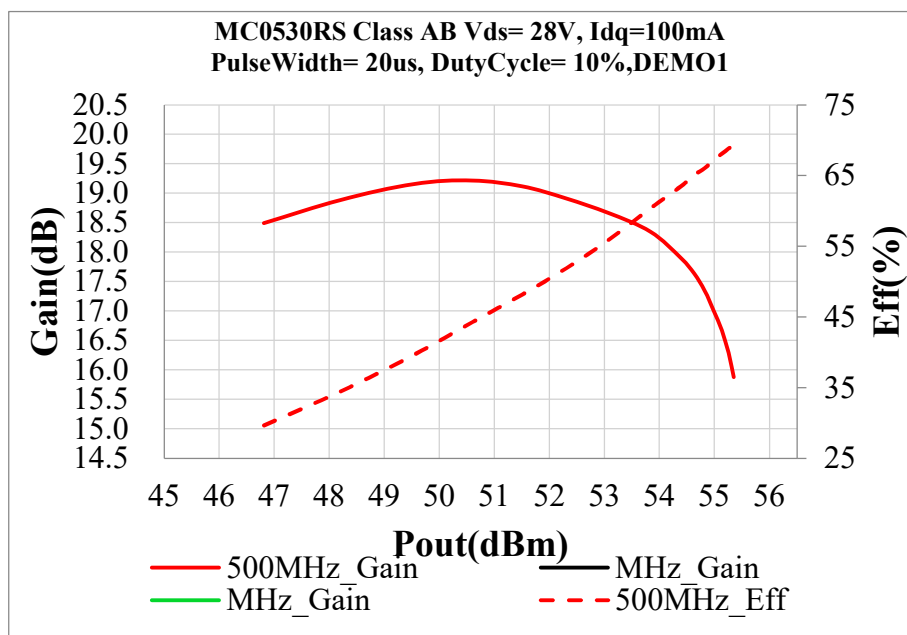
VSWR 10:1 at 300W pulse CW Output Power	No Device Degradation
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TYPICAL CHARACTERISTICS

Figure 1. Network analyzer output S11/S21 ($V_{DS}=28V, I_{DQ}=1000mA$)



Figure 2. Gain, Efficiency as function of Pout



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Figure 3. Test Circuit Component Layout

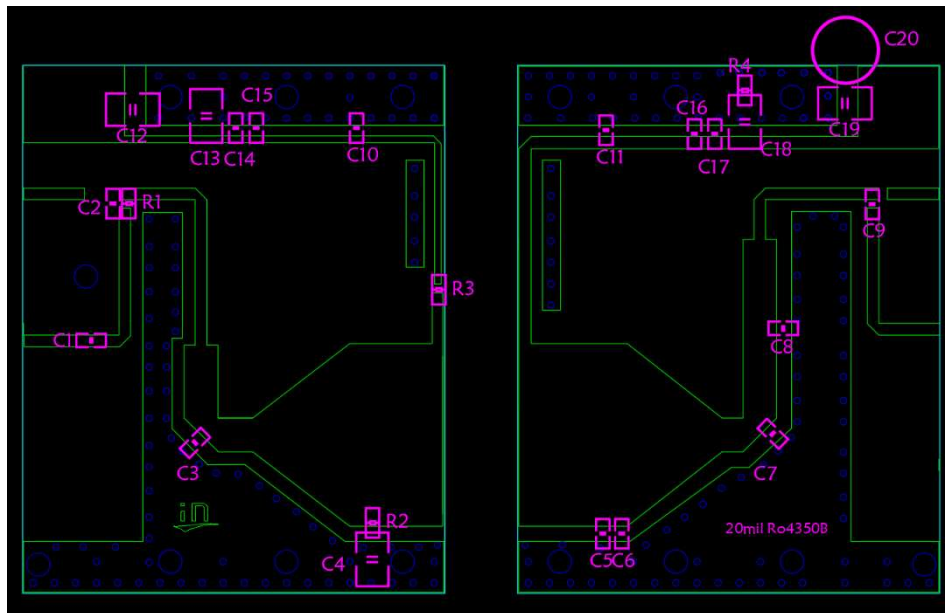


Table 5. Test Circuit Component Designations and Values

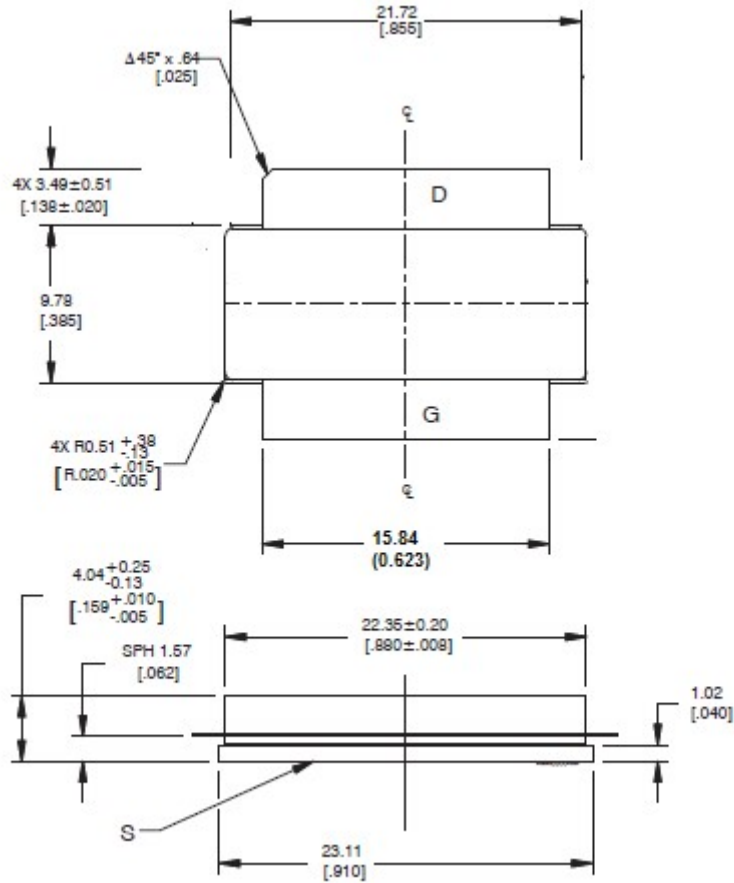
Component	Value	Quantity
U1	MC0536RS	1
C1	8.2pF	1
C2, C9, C10, C11	100pF	4
C3	43 pF	1
C5, C8	27 pF	2
C6	39pF	1
C7	18pF	1
C4, C12, C13, C18, C19	10uF/63V	5
C14, C17	10nF	2
C15, C16	1nF	2
R1	50 Ω	1
R2, R3, R4	10 Ω	3
C20	470uF/63V	1

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Package Outline

Flangeless ceramic package;



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-C2					09/27/2018

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Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2024/3/14	Rev 1.0	Product Datasheet

Application data based on ZYX-24-03

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