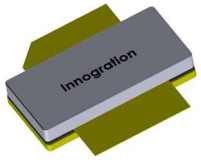
M2K1040RVS LDMOS TRANSISTORs

Document Number: M2K1040RVS
Preliminary Datasheet V1.1

400W, 0.7GHz 50V High Power RF LDMOS FETs

M2K1040RVS



Description

The M2K1040RVS is a 400watt capable, high performance, thermally enhanced，unmatched，single ended LDMOS FET, used for any frequency up to 0.7GHz,capable of delivery either CW or pulsed signal.

It is featured with high breakdown voltage and stability, and leading RF performance.

- Typical performance(on 500MHz narrow band application board with devices soldered)

M2K1040RVS Vgs=3.16V Vds=50V Idq=200mA CW								
Freq(MHz)	Pout(dBm)	Pout(W)	Idq(A)	Pin(dBm)	Gain(dB)	Eff(%)	2th(dBc)	3th(dBc)
500	56.30	423.6	12.29	38.30	18.00	69.00	-28	-38.9
500	56.15	412.1	12.00	37.30	18.85	68.68	/	/
500	56.00	398.1	11.65	36.13	19.87	68.34	/	/
500	55.78	378.4	11.16	35.13	20.65	67.82	/	/
500	55.53	357.3	10.62	34.16	21.37	67.28	/	/
500	55.19	330.4	9.98	33.13	22.06	66.21	/	/
500	54.79	301.3	9.30	32.13	22.66	64.80	/	/
500	54.24	265.5	8.54	31.12	23.12	62.17	/	/
500	53.56	227.0	7.66	30.06	23.50	59.27	/	/

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- Laser Exciter
- Synchrotron
- MRI
- Plasma generator
- Weather Radar

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	115	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case ,Case Temperature 85°C, 400W CW, 50 Vdc, Idq = 200 mA	Rth	0.19	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

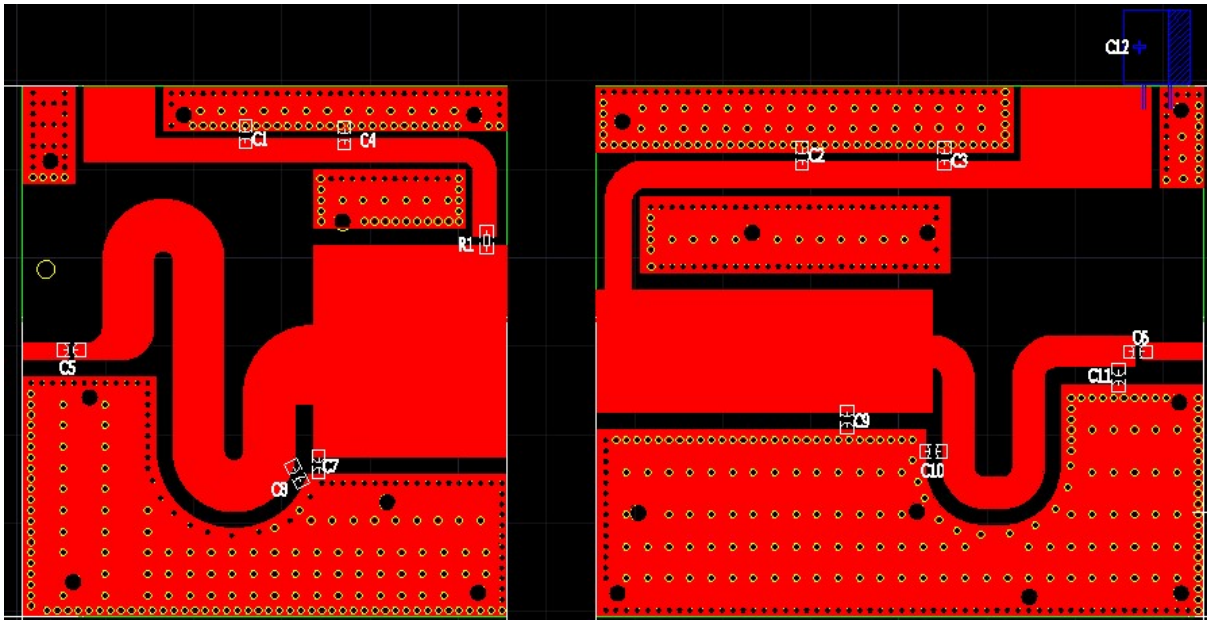
Table 4. Electrical Characteristics (T_A = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V_{GS}=0V, I_{DS}=1.0mA	$V_{(BR)DSS}$		115		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate—Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS(th)}$	——	2.54	——	V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 200 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.10	——	V
Drain source on state resistance (V_{DS} = 0.1V, V_{GS} = 10 V) Each section side of device measured	Rds(on)		55		mΩ
Common Source Input Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{ISS}		150		pF
Common Source Output Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{OSS}		60		pF
Common Source Feedback Capacitance (V_{GS} = 0V, V_{DS} =50 V, f = 1 MHz) Each section side of device measured	C_{RSS}		1.6		pF

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 50 Vdc, I_{DQ} = 200 mA, f = 500MHz, pulse width:100us, duty cycle:10%

10:1 at 400W Pulsed CW Output Power	No Device Degradation

Reference Circuit of Test Fixture (500MHz CW Power Amplifier)



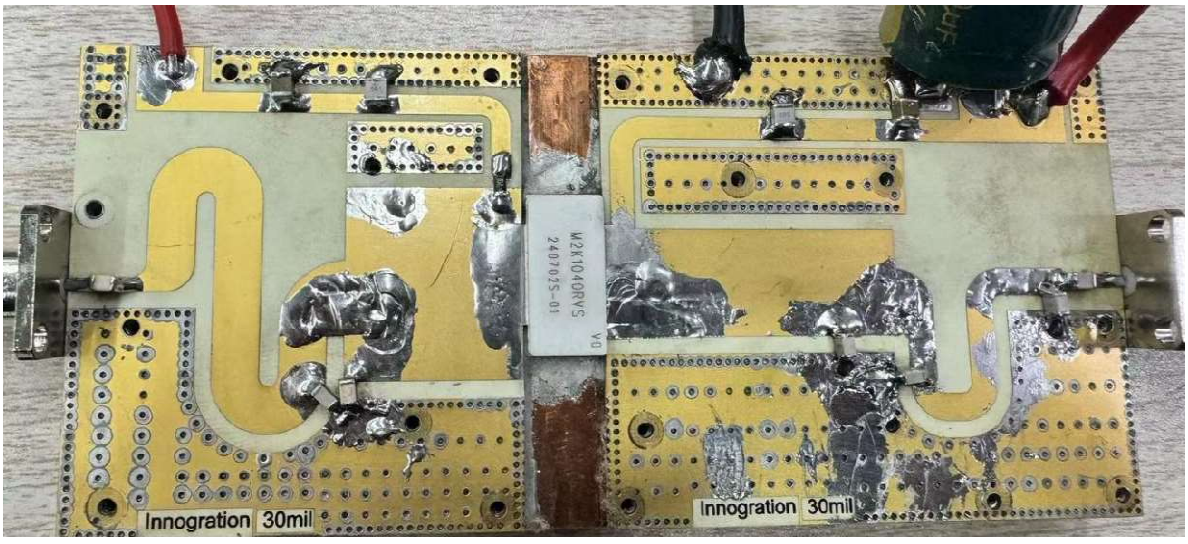
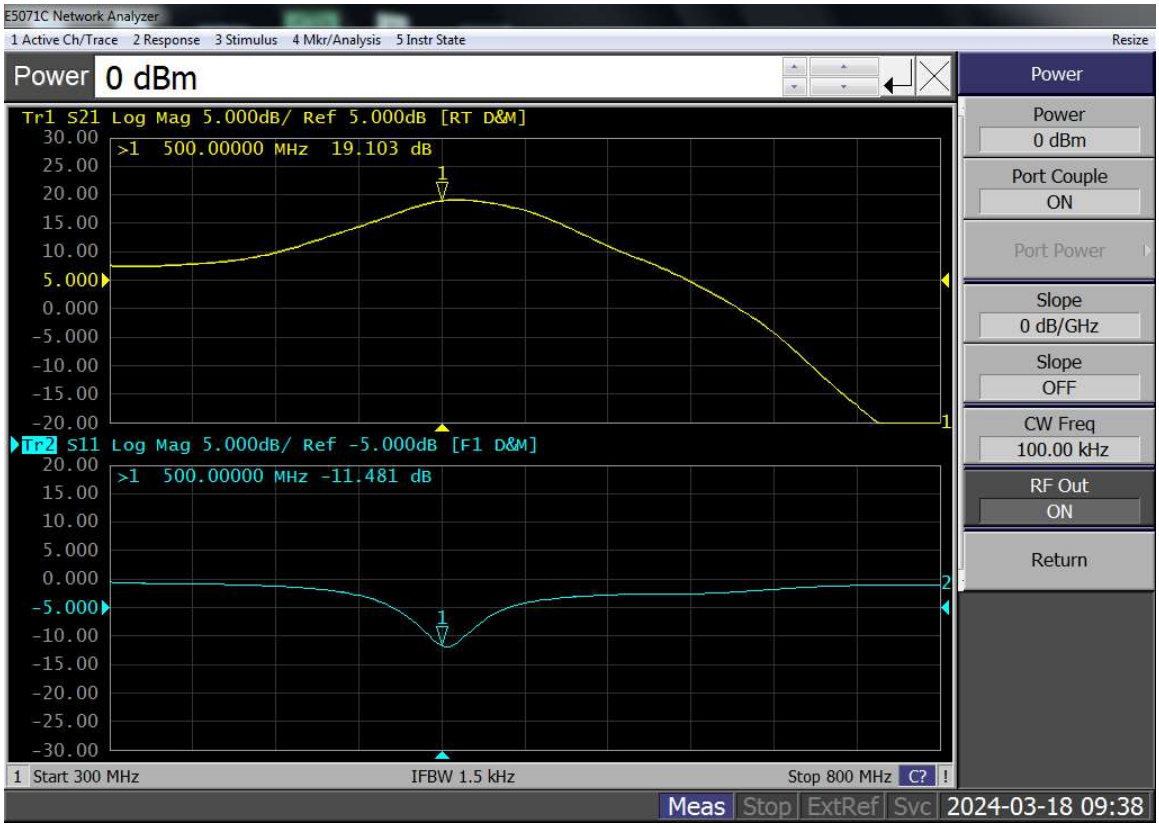


Table 5. Test Circuit Component Designations and Values

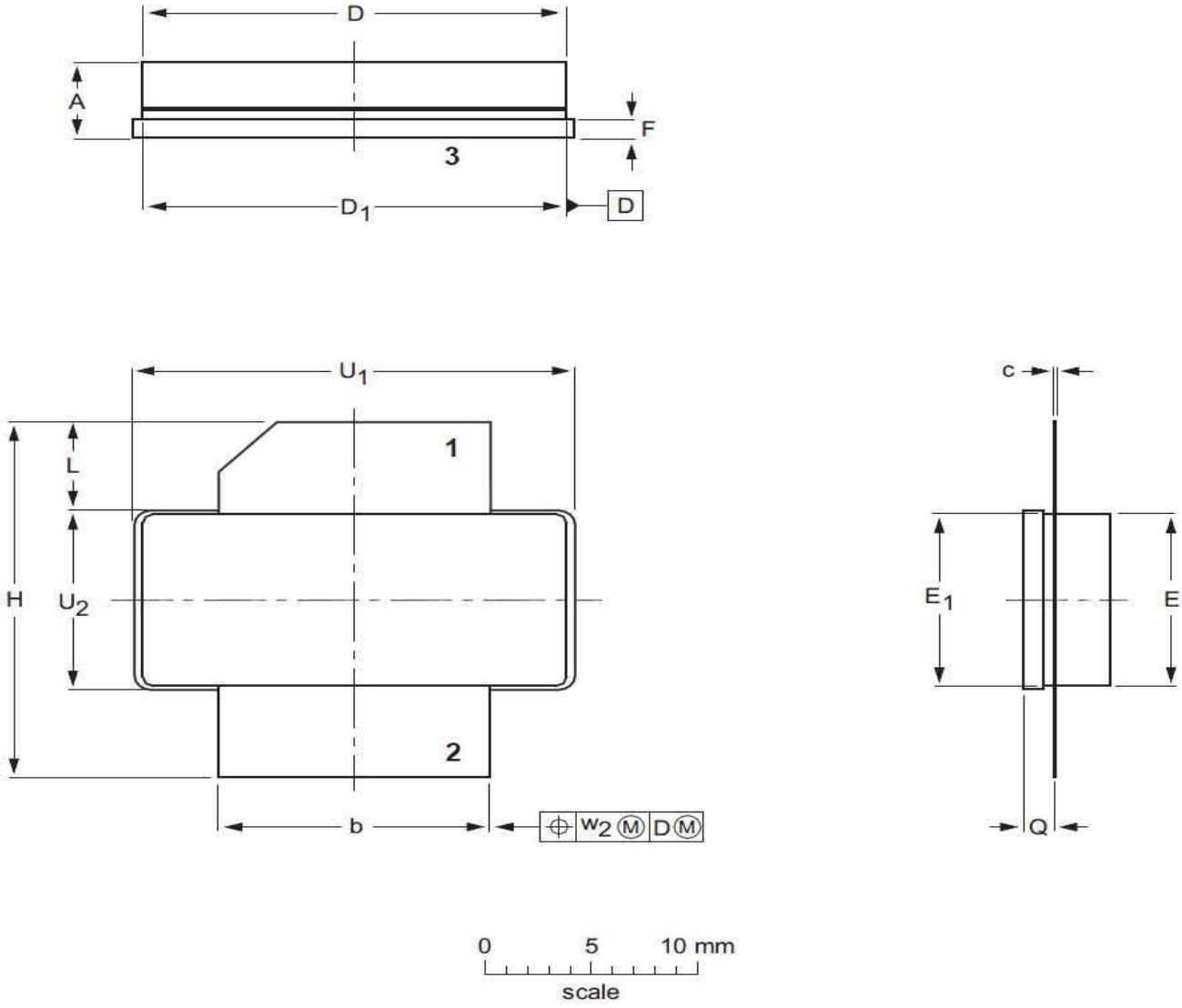
Component	Description	Suggestion
C1,C2	10uF	10uF/100V
C3~C6	560pF	MQ101111
C7	30pF	MQ101111
C8	18pF	MQ101111
C9	4.7pF	MQ101111
C10	15pF	MQ101111
C11	1pF	MQ101111
C12	4700uF/63V	Electrolytic Capacitor
R1	10 Ω	Chip Resistor
PCB	30Mil Rogers4350	

Figure 1: Network analyzer output S11/S21, Vds=50V, Idq=200mA



Package Outline

Earless flanged ceramic package; 2 leads（1—DRAIN、2—GATE、3—SOURCE）



UNIT	A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	W_2
mm	4.72	12.83	0.15	20.02	19.96	9.50	9.53	1.14	19.94	5.33	1.70	20.70	9.91	0.25
	3.43	12.57	0.08	19.61	19.66	9.30	9.25	0.89	18.92	4.32	1.45	20.45	9.65	
inches	0.186	0.505	0.006	0.788	0.786	0.374	0.375	0.045	0.785	0.210	0.067	0.815	0.390	0.010
	0.135	0.495	0.003	0.772	0.774	0.366	0.364	0.035	0.745	0.170	0.057	0.805	0.380	

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B2					03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2024/3/18	Rev 1.0	Preliminary datasheet

Application data based on HL-24-12

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