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20W,28V Plastic RF LDMOS Transistor

Description

The ITEH35020C6 is a 20-watt, highly rugged, LDMOS transistor, designed for any general applications at frequencies 2.7 to 3.5GHz, in 10*6mm QFN plastic package, supporting surface mounted on PCB through high density grounding vias.

It is part of low power general purpose plastic LDMOS with pin to pin compatibility.

•Typical 2.7-3.5GHz Class AB RF Performance (On Innogration fixture with device soldered).

VDS=28V. IDQ=10mA. Vgs=2.4V

DS- 26V , IDQ-10HA, VgS-2.4V							
Freq	P1dB	P1dB	P1dB	P1dB	P3dB	P3dB	P3dB
(MHz)	(dBm)	(W)	Eff(%)	Gain(dB)	(dBm)	(W)	Eff(%)
2700	44. 23	26. 5	53.5	12.6	44. 91	31.0	54. 9
2800	44. 27	26.7	51.9	12.9	45. 01	31. 7	53.9
2900	44. 26	26. 7	50.9	13. 18	45	31.6	52.8
3000	44. 19	26. 2	50.8	13. 51	44. 96	31.3	53.0
3100	44. 14	25.9	51.8	13.65	44. 86	30.6	53. 5
3200	43.96	24.9	52.5	13.61	44. 65	29. 2	53.6
3300	43.51	22.4	51.7	13. 47	44. 21	26. 4	52.4
3400	43. 2	20.9	50.2	13. 15	44. 09	25. 7	52.6
3500	43.09	20.4	52.7	13.05	43. 76	23.8	53. 5

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

• S band pulse power amplifier

Table 1. Maximum Ratings

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Rating	Symbol	Value	Unit	
DrainSource Voltage	V _{DSS}	+65	Vdc	
GateSource Voltage	V _{GS}	-10 to +10	Vdc	
Operating Voltage	V_{DD}	+28	Vdc	
Storage Temperature Range	Tstg	-65 to +150	°C	
Case Operating Temperature	Tc	+150	°C	
Operating Junction Temperature	T,	+225	°C	

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	Rелс	0.0	°C/W
T _C = 85°C, T _J =200°C, DC test		0.9	

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Table 3. ESD Protection Characteristics

Test Methodology	Class	
Human Body Model (per JESD22A114)	Class 2	

Table 4. Electrical Characteristics (TA = 25 $^{\circ}$ C unless otherwise noted)

Characteristic	Symbol	Min	Тур	Max	Unit
DC Characteristics					
Drain-Source Voltage	V		GE.		V
V _{GS} =0, I _{DS} =100uA	V _{(BR)DSS}		65		V
Zero Gate Voltage Drain Leakage Current				1	
$(V_{DS} = 28V, V_{GS} = 0 V)$	Ipss			I	μΑ
GateSource Leakage Current				1	
$(V_{GS} = 11 \text{ V}, V_{DS} = 0 \text{ V})$	Igss			Į.	μΑ
Gate Threshold Voltage	\/ (41-)		2		V
$(V_{DS} = 28V, I_D = 600 \mu A)$	V _{GS} (th)		2		V
Gate Quiescent Voltage	V		2.7		V
(V _{DD} = 28V, I _D = 160mA, Measured in Functional Test)	$V_{GS(Q)}$		2.1		V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): $V_{DD} = 28 Vdc$, $I_{DQ} = 100 mA$, f = 3600 MHz

SWR 10:1 at 20W pulse CW Output Power	No Device Degradation
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Figure 1:Pin Definition(Top View)



Pin No.	Symbol	Description
8,9,10,11	Vgs/RF In	Vgs and RF input
32,33,34,35	Vds/RF out	Vds and RF output
2,5,7,12,13,18,20,23,25,30,31,36	GND	DC/RF Ground
Others	NC	No connection
Package Base	GND	DC/RF Ground.



Reference Circuit of Test Fixture Assembly Diagram 2700-3500MHz RO4350B 20mils

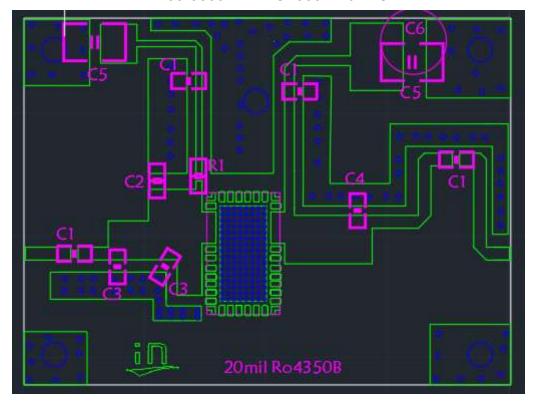


Figure 2. Test Circuit Component Layout

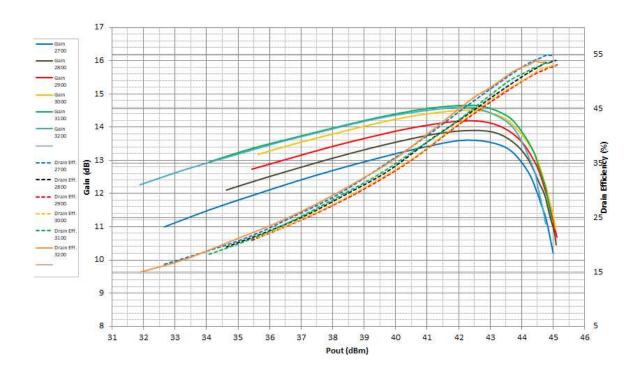
Table 5. Test Circuit Component Designations and Values

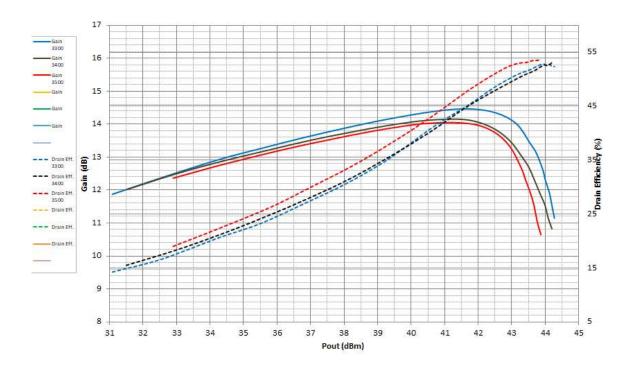
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Component	Value	Quantity		
C1	8.2pF	4		
C2	0.3pF	1		
R1	10 ohm	1		
C3	0.5pF	2		
C4	1.1pF	1		
C5	10uF/63V	2		
C6	470uF	1		



TYPICAL CHARACTERISTICS

Figure 3. Power Gain and Drain Efficiency as function of Power Out







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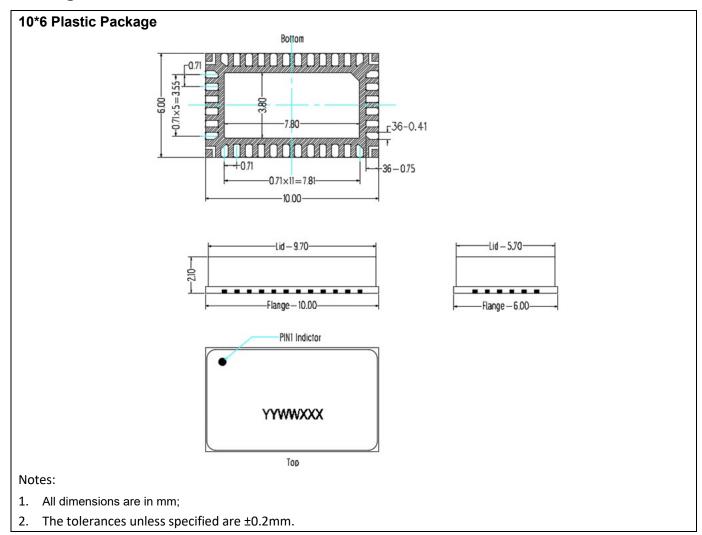


Figure 4.Network analyzer output S11/S21



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Package Dimensions



Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2024/3/21	Rev 1.0	Preliminary Datasheet

Application data based on ZXY-24-6

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