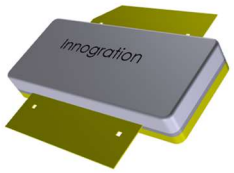
2900MHz, 350W, 32V High Power RF LDMOS FETs

ITCH29350C2



Description

The ITCH29350C2 is a 350-watt, internally matched LDMOS FETs, designed for multiple applications with frequencies at 2900MHz for ISM and RF Energy applications

- Typical Performance in 2.8/2.9G application boards with devices soldered

V_{DS}=32V,I_{DQ}=500mA, Pulsed CW 10% 25us

Freq	P1dB	P1dB	P1dB Eff	P1dB Gain	P3dB	P3dB	P3dB Eff
(MHz)	(dBm)	(W)	%	dB	(dBm)	(W)	%
2900	55.28	337.62	43	10	56.0	400	45

Freq	P1dB	P1dB	P1dB Eff	P1dB Gain	P3dB	P3dB	P3dB Eff
(MHz)	(dBm)	(W)	%	dB	(dBm)	(W)	%
2800	55.06	320.55	42	9.9	55.94	392.37	45

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Internally Matched for Ease of Use
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	70	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+32	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 350W Pulsed Output	$R_{\theta JC}$	0.1	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Breakdown Voltage (V_{GS}=0V; I_D=100uA)	V_{DSS}	65	70	——	V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 V, V_{GS} = 0 V)	I_{DSS}	——	——	10	μA
Gate--Source Leakage Current (V_{GS} = 6 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 28V, I_D = 600 uA)	$V_{GS(th)}$	——	1.9	——	V
Gate Quiescent Voltage (V_{DS} = 28 V, I_{DQ} = 500 mA, Measured in Functional Test)	$V_{GS(Q)}$		3	3.5	V

Functional Tests (In Innogration Test Fixture, 50 ohm system) : V_{DS} = 32 Vdc, I_{DQ} = 500 mA, f = 2900 MHz, Pulse CW Signal Measurements.

(Pulse Width=20 μs, Duty cycle=10%)

Power Gain @ P_{3dB}	Gp	8	9	——	dB
Drain Efficiency@P3dB	η_D	43	45	——	%
3dB Compression Point	P_{-3dB}	350	400	——	W
Input Return Loss	IRL	——	-7	——	dB

Load Mismatch of per Section (On Test Fixture, 50 ohm system): V_{DD} = 32 Vdc, I_{DQ} = 500 mA, f = 2900 MHz

VSWR 5:1 at 350W pulse CW Output Power	No Device Degradation

2900MHz
Reference Circuit of Test Fixture Assembly Diagram

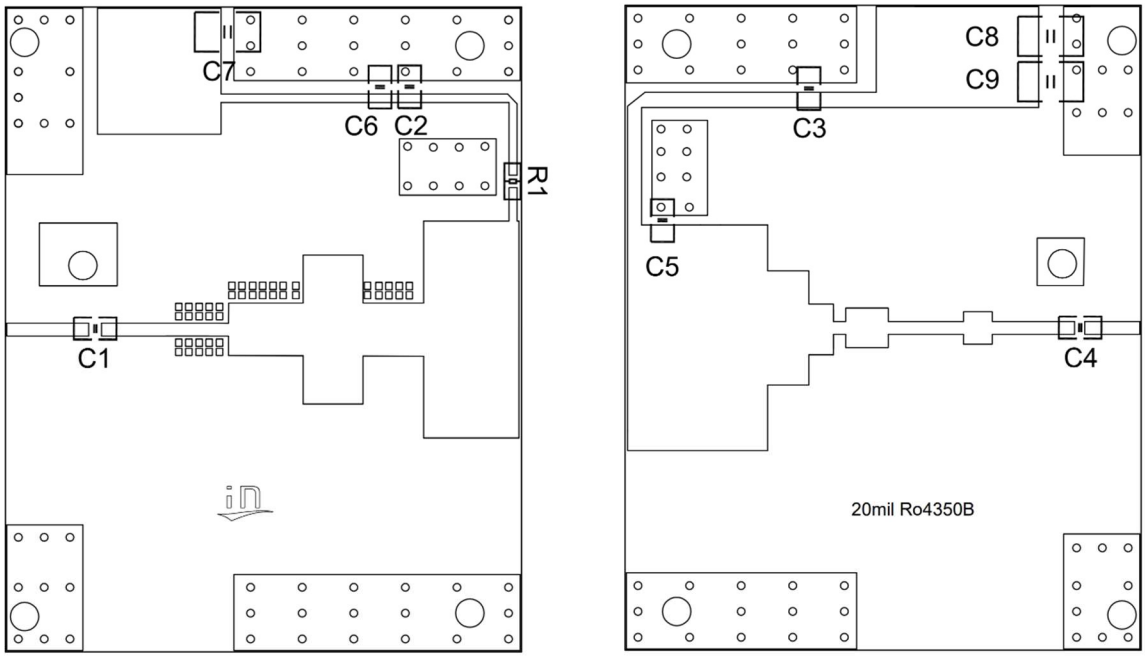


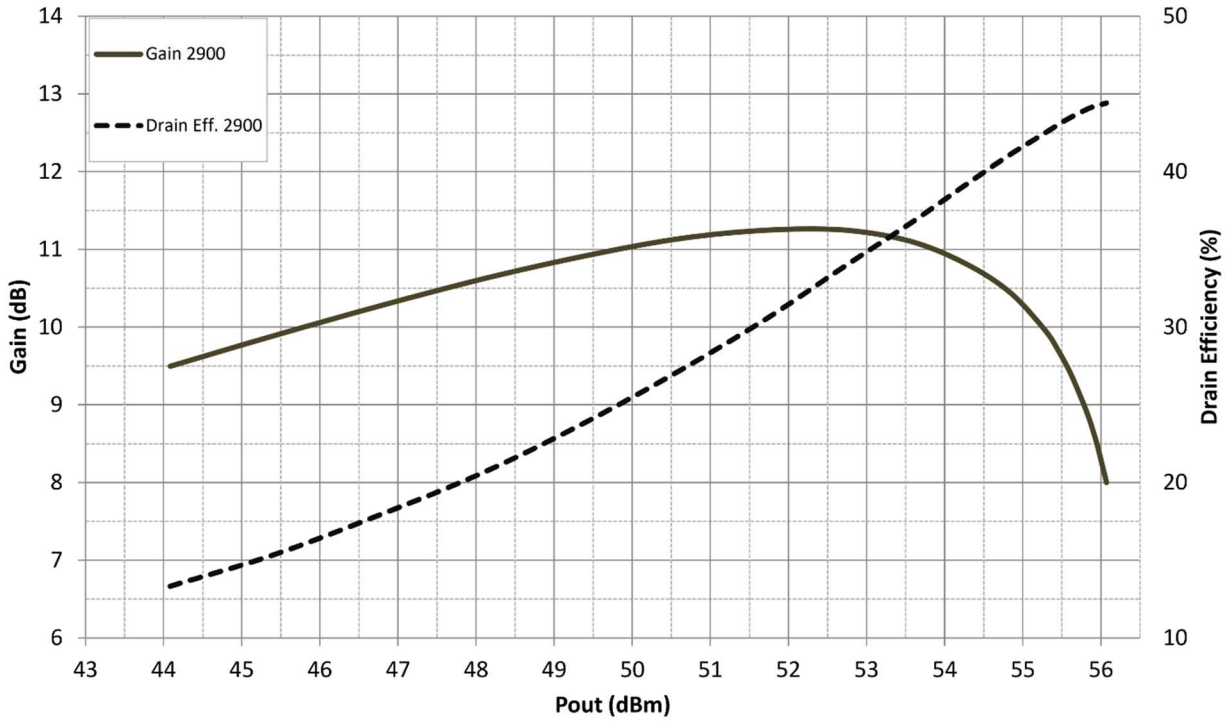
Figure 1. Test Circuit Component Layout (2900MHz)

Table 1. Test Circuit Component Designations and Values

Reference	Footprint	Value	Quantity
C1, C2, C3, C4,	0805	15pF/250V	4
C5	0805	0.5pF/250V	1
C6	0805	1uF/50V	1
C7, C8, C9	1210	10uF/100V	3
R1	0603	10R	1
U1	C6	ITCH29350C2	1

TYPICAL CHARACTERISTICS

Figure 2. Power Gain and Drain Efficiency as Function of Pulsed CW Output Power



2800MHz

Reference Circuit of Test Fixture Assembly Diagram

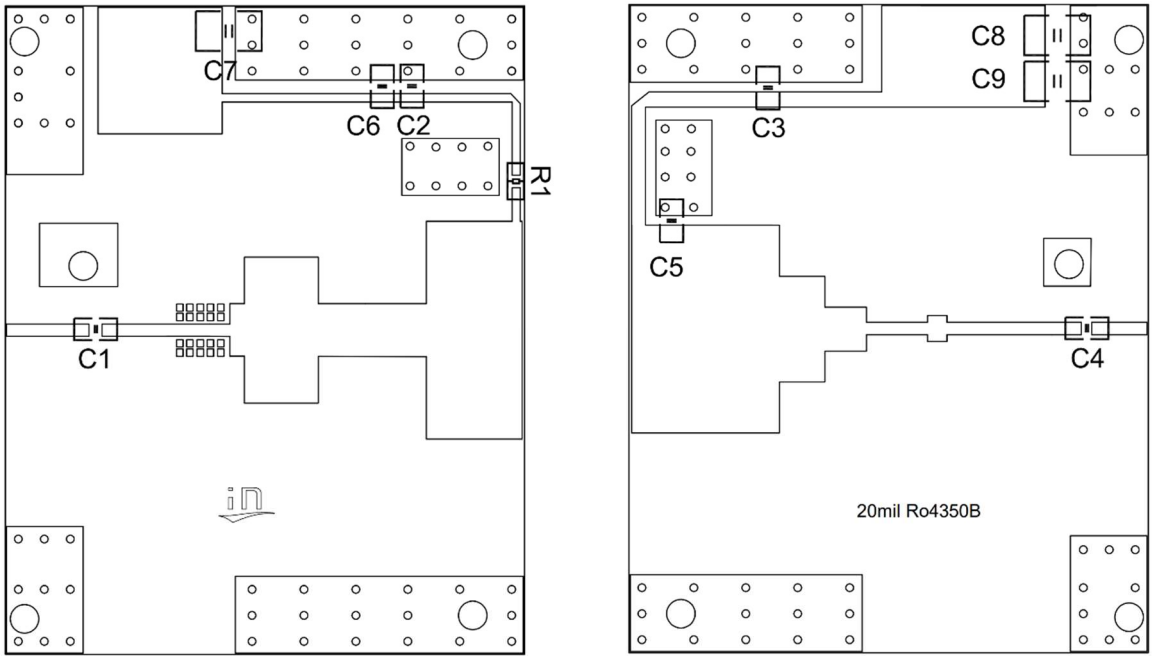


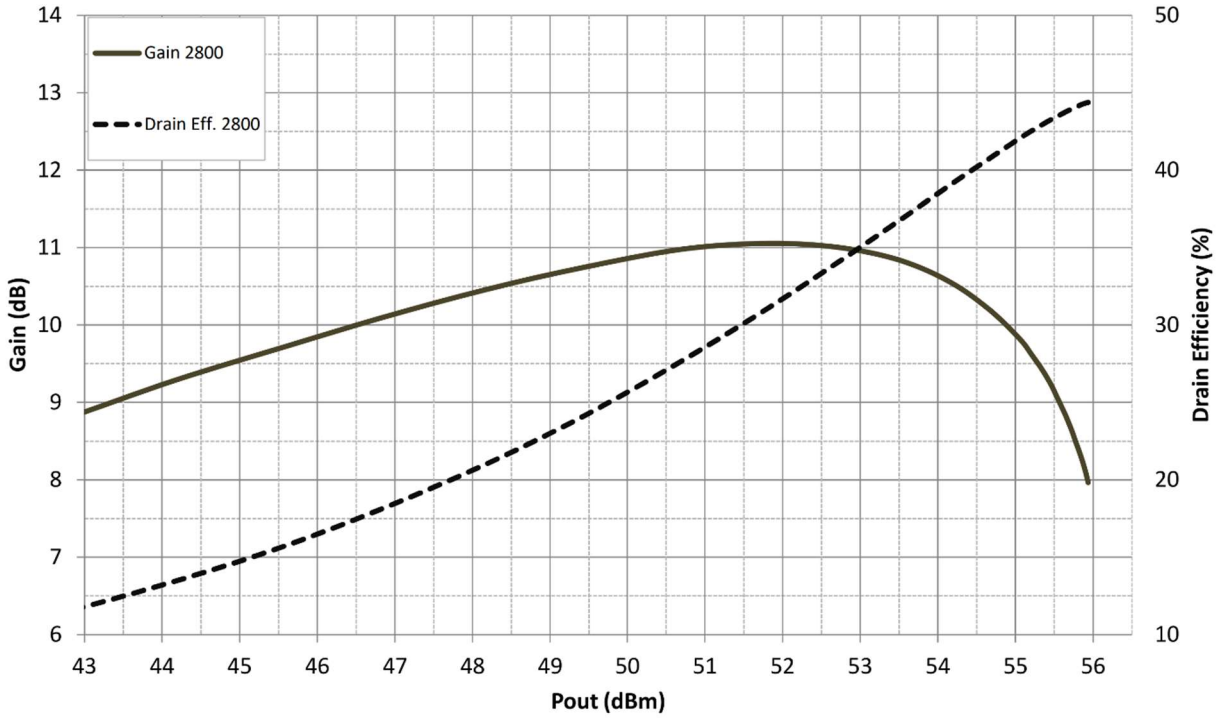
Figure 3. Test Circuit Component Layout (2800MHz)

Table 6. Test Circuit Component Designations and Values

Reference	Footprint	Value	Quantity
C1, C2, C3, C4,	0805	15pF/250V	4
C5	0805	0.5pF/250V	1
C6	0805	1uF/50V	1
C7, C8, C9	1210	10uF/100V	3
R1	0603	10R	1
U1	C2	ITCH29350C2	1

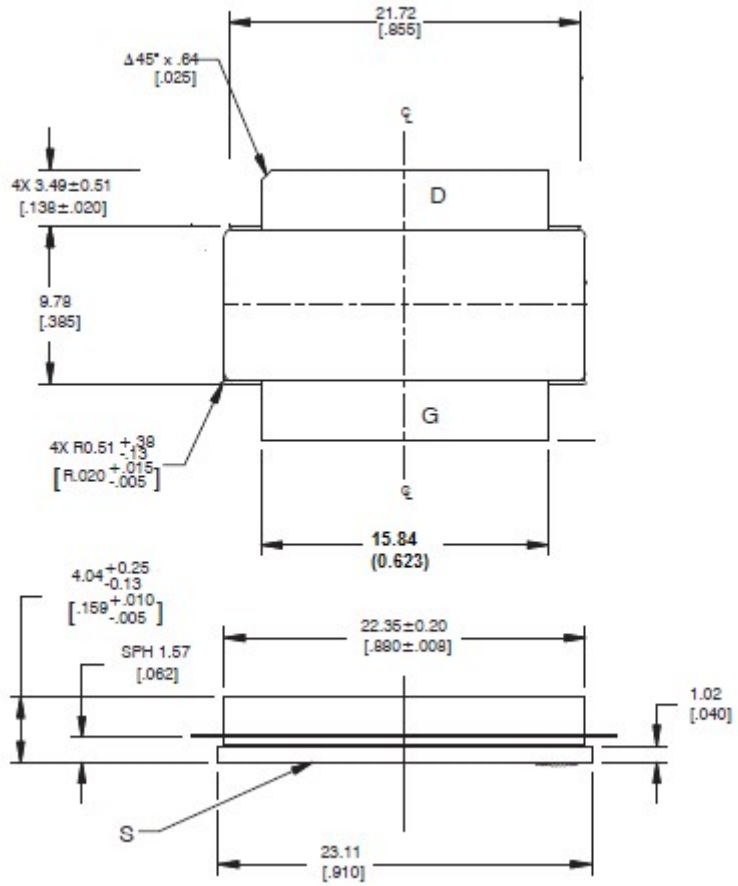
TYPICAL CHARACTERISTICS

Figure 3. Power Gain and Drain Efficiency as Function of Pulsed CW Output Power



Package Outline

Flangeless ceramic package;



OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-C2					09/27/2018

Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2024/3/22	**V1.0**	**Preliminary Datasheet Creation**

Application data based on ZBB-24-08/10

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