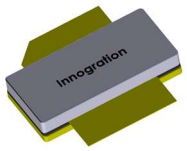
ITGV10220BY2 LDMOS TRANSISTOR

Document Number: ITGV10220BY2
Product Datasheet V1.0

220W, 50V High Power RF LDMOS FETs

ITGV10220BY2



Description

The ITGV10220BY2 is a 220-watt capable, high performance, input matched LDMOS FET, designed for UHF band up to 1GHz. It can be used for both CW and pulse application.

It is featured for high power and high ruggedness, low cost, suitable for ISM RF Energy application especially 915MHz etc

- Typical Performance (On Innogration 915MHz fixture with device soldered):

V_{DS}= 50V, Idq=10mA，CW

Freq (MHz)	Pin (dBm)	Gain (dB)	Pout (W)	P3dB Eff(%)
915	32.2	21	230	69

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- high stability and ruggedness
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Excellent thermal stability, low HCI drift
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	110	Vdc
Gate--Source Voltage	V_{GS}	-7 to +10	Vdc
Operating Voltage	V_{DD}	+50	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case ,Case Temperature 80°C, 220W CW, 50 Vdc, I_{DQ} = 100 mA	$R_{\theta JC}$	0.7	°C/W

Table 3. ESD Protection Characteristics

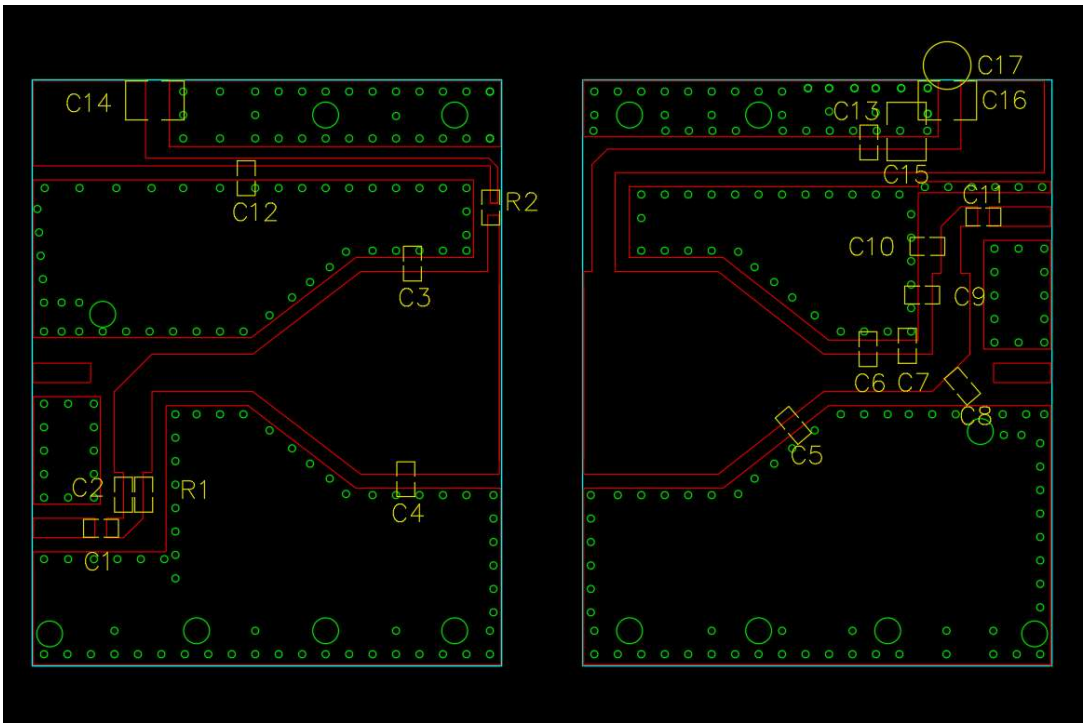
Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics (Per Side)					
Drain-Source Voltage V_{GS}=0, I_{DS}=18.0mA	$V_{(BR)DSS}$	110			V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50V, V_{GS} = 0 V)	I_{DSS}			1	μA
Gate—Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}			1	μA

Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS(th)}$		2.6		V
Gate Quiescent Voltage (V_{DD} = 50 V, I_D = 100 mA, Measured in Functional Test)	$V_{GS(Q)}$		3.1		V

Reference Circuit of Test Fixture (915MHz)



Component	Value	Quantity
U1	ITGV10220BY2	1
C1	5.6pF	1
C2、C11、C12、C13	68pF	4
C3、C5	10pF	2
C4	15pF	1
C6、C7	4.7pF	2
C8	2pF	1
C9	1pF	1
C10	0.5pF	1
C14、C15、C16	10uF/63V	3
C17	470uF/63V	1
R1	50 Ω	1
R2	10 Ω	1

TYPICAL CHARACTERISTICS

Figure 1. Power Gain and Drain Efficiency as Function of Pulsed CW Output Power

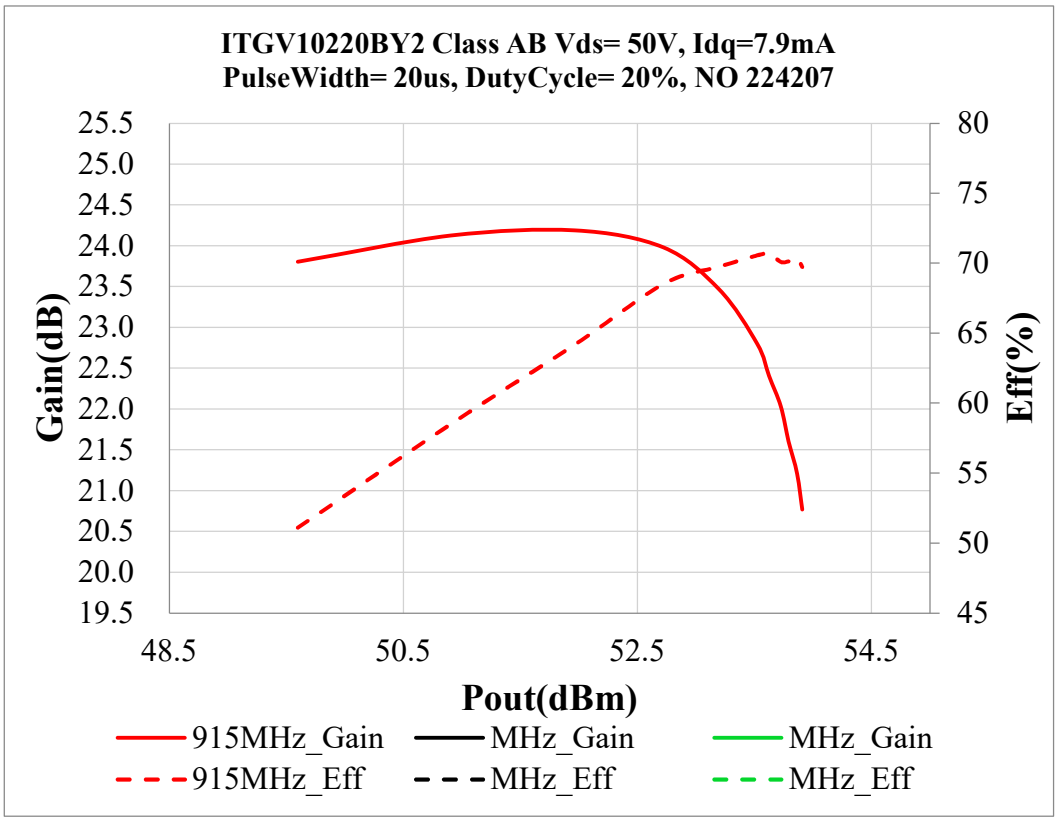
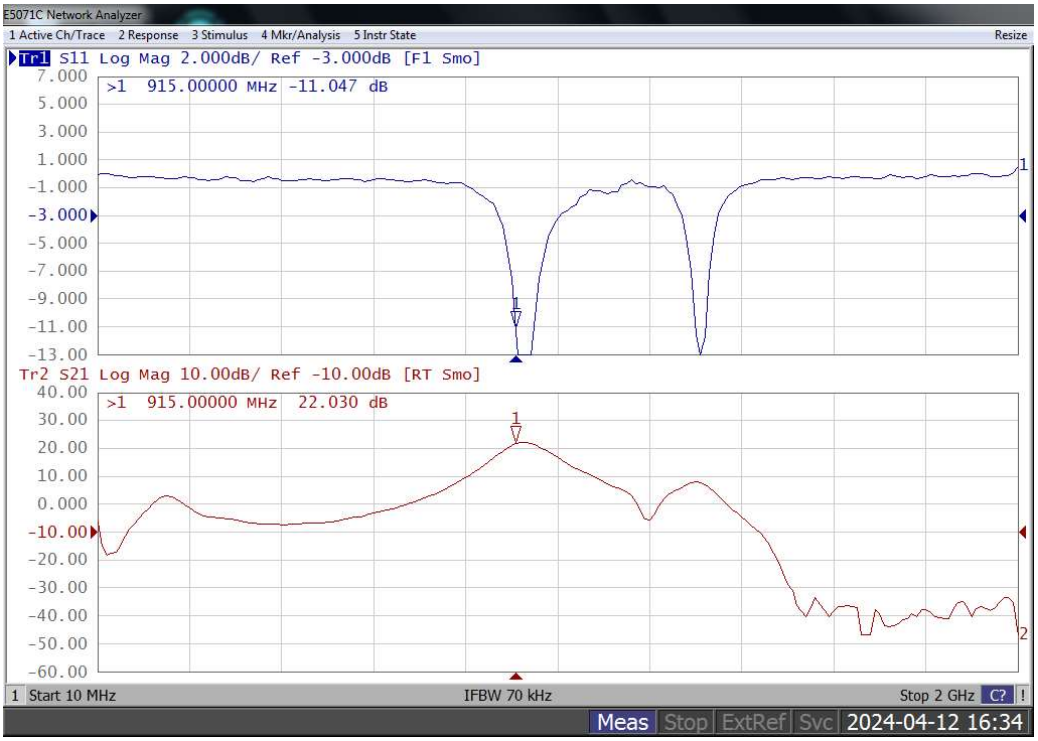
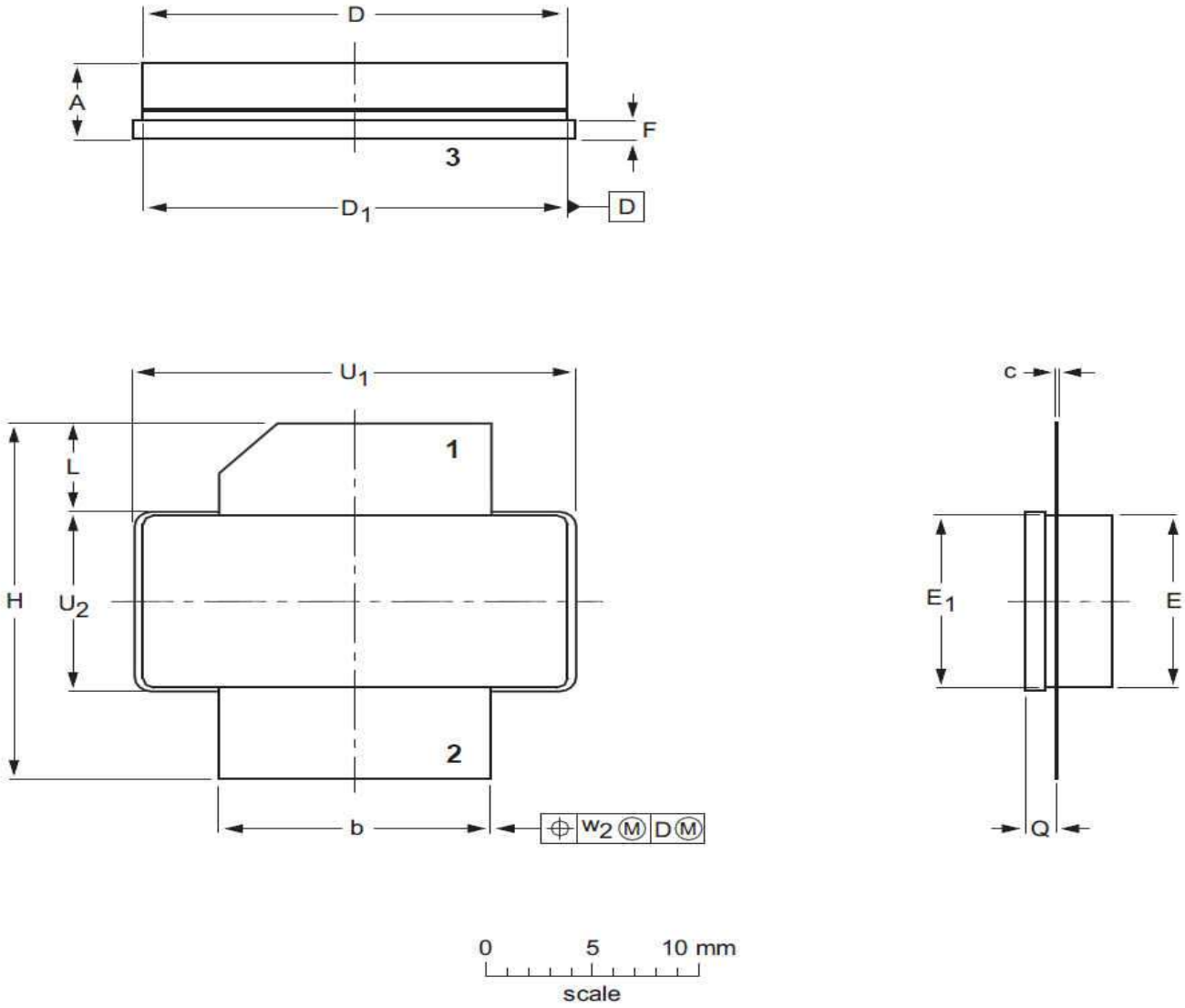


Figure 3. Network analyzer Output S11/S21



Package Outline

Earless flanged ceramic package; 2 leads（1—DRAIN、2—GATE、3—SOURCE）



UNIT	A	b	c	D	D_1	E	E_1	F	H	L	Q	U_1	U_2	W_2
mm	4.72 3.43	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.53 9.25	1.14 0.89	19.94 18.92	5.33 4.32	1.70 1.45	20.70 20.45	9.91 9.65	0.25
inches	0.186 0.135	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.375 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.067 0.057	0.815 0.805	0.390 0.380	0.010

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-B2					03/12/2013

Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2024/4/12	Rev 1.0	Preliminary Datasheet

Application data based on ZYX-24-32

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