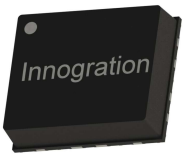
ITEV05220C9 LDMOS TRANSISTOR

Document Number: ITEV05220C9
Preliminary Datasheet V1.0

220W,50V High Power RF LDMOS FETs

ITEV05220C9



Description

The ITEV05220C9 is a 220watt capable, high performance, internally matched LDMOS FET, designed for RF Energy or ISM application centered at 433MHz, in cost effective 12*10mm QFN plastic package,

It can be soldered on PCB through high density grounding vias or soldered directly on heatsink, according to different applications.

- Typical CW performance(on Innogration test board with device soldered on heatsink directly)

50V, Idq=1mA

Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
433	52.8	190.6	72.6	21.24	53.47	222.5	74

40V, Idq=1mA

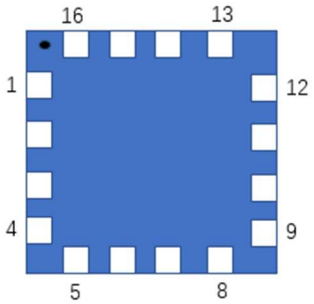
Freq (MHz)	P1dB (dBm)	P1dB (W)	P1dB Eff(%)	P1dB Gain(dB)	P3dB (dBm)	P3dB (W)	P3dB Eff(%)
433	50.94	124.0	74	20.2	51.62	145.3	75

Recommended driver: ITGV22010C6

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Pin Configuration and Description （Top view）



Pin No.	Symbol	Description
5-8	RF IN/Vgs	RF Input/Gate bias
13-16	RF OUT/Vds	RF Output/Drain bias
Others	NC	Can be left as either no use or grounding
Package Base	GND	DC/RF Ground. Proposed to be soldered to heatsink plane directly for the best CW thermal and RF performance. Soldered through vias or copper coin allowed for pulsed CW applications, but will result in excessive junction temperatures and different RF performance

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+110	Vdc
Gate--Source Voltage	V_{GS}	-10 to +10	Vdc
Operating Voltage	V_{DD}	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T_C= 85°C, T_J=200°C, DC test, soldered on heatsink	RθJC	0.7	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (T_A = 25 ℃ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics (per half section)					
Drain-Source Voltage V_{GS}=0, I_{DS}=1.0mA	$V_{(BR)DSS}$		110		V
Zero Gate Voltage Drain Leakage Current (V_{DS} = 75V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Zero Gate Voltage Drain Leakage Current (V_{DS} = 50V, V_{GS} = 0 V)	I_{DSS}	——	——	1	μA
Gate--Source Leakage Current (V_{GS} = 10 V, V_{DS} = 0 V)	I_{GSS}	——	——	1	μA
Gate Threshold Voltage (V_{DS} = 50V, I_D = 600 μA)	$V_{GS(th)}$	——	2.65	——	V
Gate Quiescent Voltage (V_{DD} =50 V, I_D = 200 mA, Measured in Functional Test)	$V_{GS(Q)}$	——	3.4	——	V

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V_{DD} = 50 Vdc, I_{DQ} = 200 mA, f =433MHz, pulse width:100us, duty cycle:10%

Load 10:1 All phase angles, at 220W Pulsed CW Output Power	No Device Degradation

TYPICAL CHARACTERISTICS

Figure 1: CW Gain and Power Efficiency as a Function of Pout at 433MHz

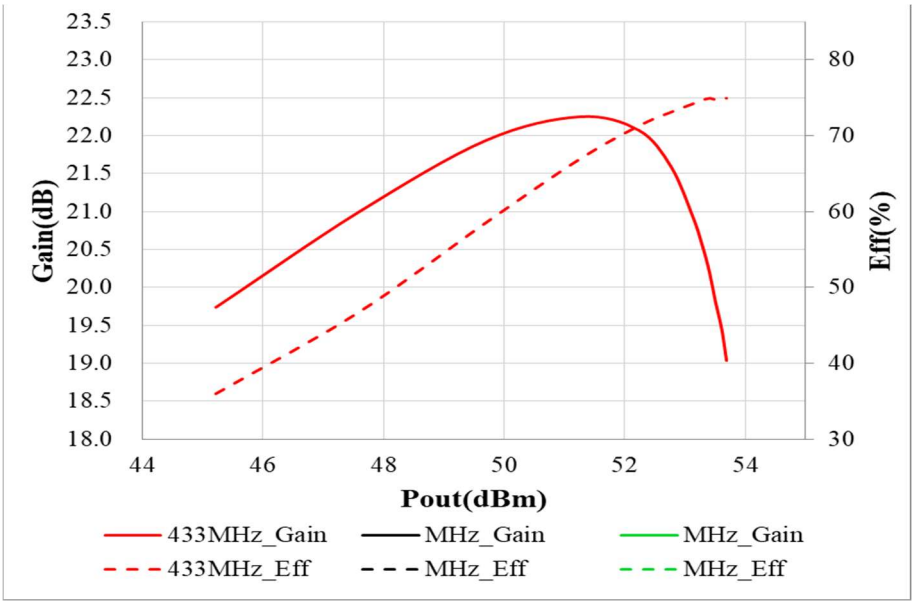
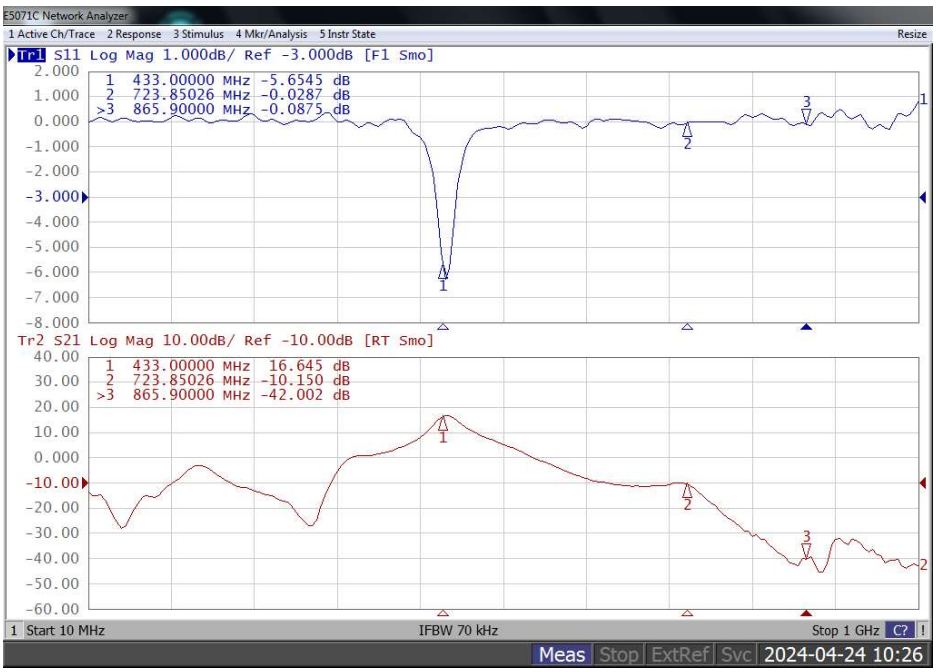


Figure 2: Network analyzer output S11/221



Reference Circuit of Test Fixture Assembly Diagram

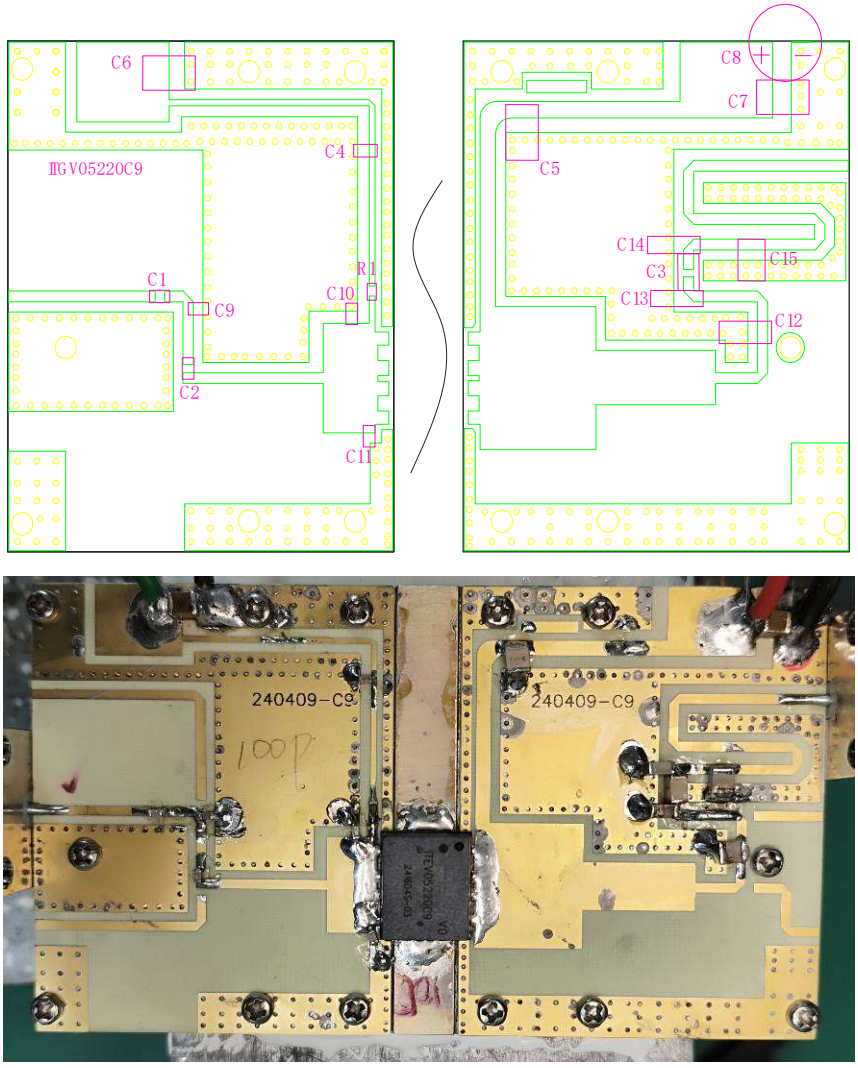
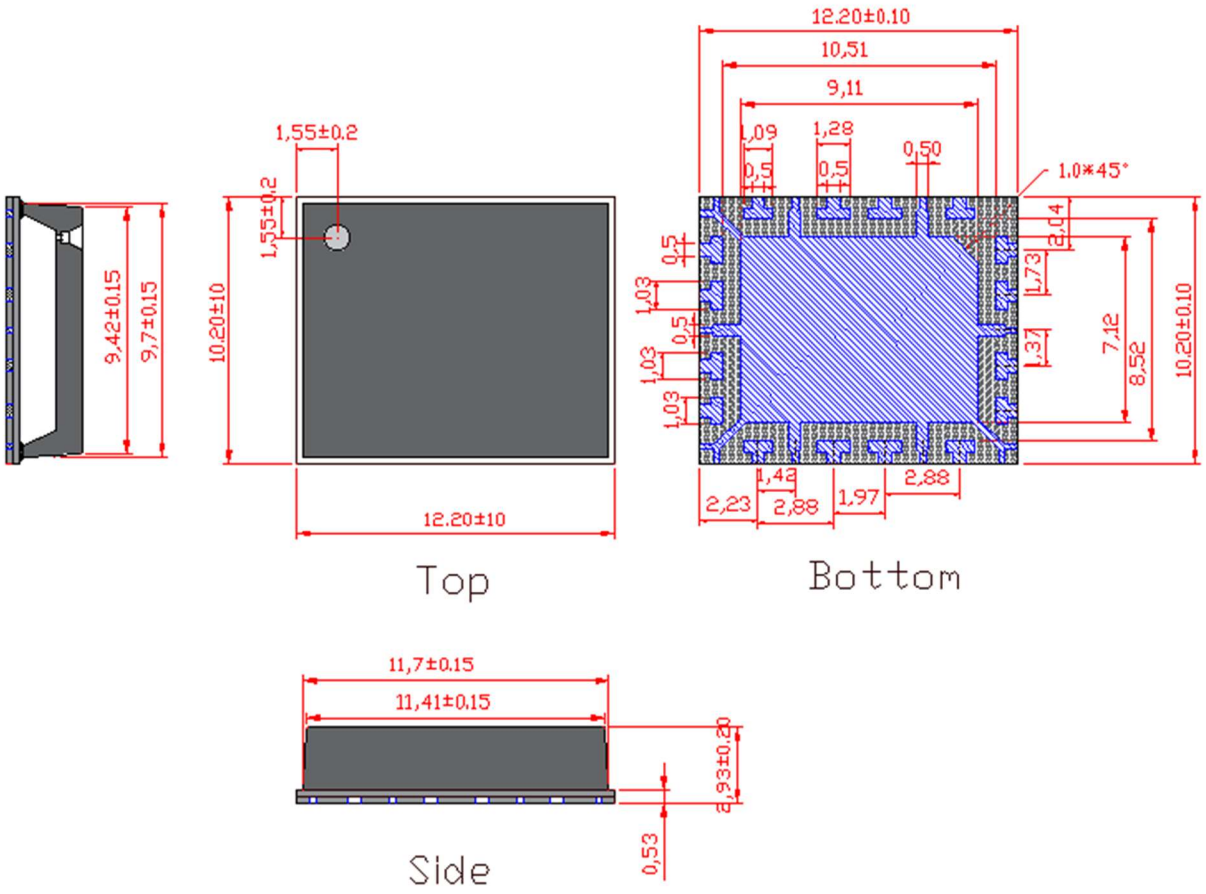


Table 5. Test Circuit Component Designations and Values

Designator	Comment	Footprint	Quantity
C1	3.9 pF(High Q)	0603/0805	1
C2, C4	100 pF (High Q)	0603/0805	2
C3, C5	100 pF (High Q)	1210	2
C6, C7	10 uF/100V	1210	2
C8	470 uF/63V		1
R1	10 Ω	0603	1
C9, C11	20 pF (High Q)	0603/0805	2
C10	30 pF (High Q)	0603/0805	1
C12	1.5 pF (High Q)	1210	1
C13, C14	3.9 pF (High Q)	1210	2
C15	10 pF (High Q)	1210	1

Package Dimensions （Unit:mm）



Revision history

Table 5. Document revision history

Date	Revision	Datasheet Status
2024/4/24	Rev 1.0	Preliminary Datasheet Creation

Application data based on LSM-24-13

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