# 400W, HF-150MHz 50V High Power RF LDMOS

# **Description**

The MV0545VX is a 400W single ended 50V LDMOS, unmatched for any applications within HF-150MHz

It supports CW, and pulsed and any modulated signal at either saturated or linear application.

# It can be the drop-in replacement of its equivalent 400W single ended VDMOS like SD2943 etc with improved RF performance like higher efficiency

Typical performance(on Innogration test board with device soldered)
Signal: CW , Vgs=3.2v,Vds=50v,Idq=200mA

Freq(MHz)	Pin(dBm)	Pout(dBm)	Pout(W)	lds(A)	Gain(dB)	Eff(%)	2 <sup>nd</sup>	3 <sup>rd</sup>
rieq(Wiriz)	Fili(dbili)	Fout(dBill)	Foul(vv)	ius(A)	Gain(dB)		Harmonic(dB)	Harmonic(dB)
30	31.3	56.3	430	11.4	25	75	-29	-25

### **Features**

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- · Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

# **Suitable Applications**

- 30-88MHz (Ground communication)
- 54-88MHz (TV VHF I)
- 88-108MHz (FM)
- 160-230MHz (TV VHF III)
- 136-174MHz (Commercial ground communication)
- Laser Exciter
- Synchrotron
- MRI
- Plasma generator
- Weather Radar

### **Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
DrainSource Voltage	V <sub>DSS</sub>	+135	Vdc
GateSource Voltage	V <sub>GS</sub>	-10 to +10	Vdc
Operating Voltage	V <sub>DD</sub>	+55	Vdc
Storage Temperature Range	Tstg	-65 to +150	°C
Case Operating Temperature	Tc	+150	°C
Operating Junction Temperature	TJ	+225	°C

### **Table 2. Thermal Characteristics**

Characteristic	Symbol	Value	Unit	
Thermal Resistance, Junction to Case	Paus	0.27	OCAM.	
T <sub>C</sub> = 85°C, T <sub>J</sub> =200°C, DC test	R⊕JC	0.27	°C/W	

### **Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22A114)	Class 2

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Table 4. Electrical Characteristics ( $T_A = 25$  °C unless otherwise noted)

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Characteristic	Symbol	Min	Тур	Max	Unit
DC Characteristics					
Drain-Source Voltage	V		405		V
$V_{GS}$ =0, $I_{DS}$ =1.0mA	V <sub>(BR)DSS</sub>		133		
Zero Gate Voltage Drain Leakage Current	I <sub>pss</sub>			1	μА
$(V_{DS} = 75V, V_{GS} = 0 V)$	IDSS				
Zero Gate Voltage Drain Leakage Current				1	
$(V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V})$	I <sub>DSS</sub>			I	μА
GateSource Leakage Current	I <sub>GSS</sub>			1	
$(V_{GS} = 10 \text{ V}, V_{DS} = 0 \text{ V})$	IGSS			ı	μА
Gate Threshold Voltage	V <sub>GS</sub> (th)		2.65		V
$(V_{DS} = 50V, I_D = 600 \mu A)$	V <sub>GS</sub> (th)				
Gate Quiescent Voltage	$V_{GS(Q)}$		2.2		V
$(V_{DD}$ = 50 V, $I_D$ = 200 mA, Measured in Functional Test)	V <sub>GS(Q)</sub>		3.2		V
Drain source on state resistance	Rds(on)		05		mΩ
(Vds=0.1V, Vgs=10V)	(Nus(OII)		95		11152
Common Source Input Capacitance			240		25
$(V_{GS} = 0V, V_{DS} = 50 V, f = 1 MHz)$	C <sub>ISS</sub>		340		pF
Common Source Output Capacitance			00		pF
$(V_{GS} = 0V, V_{DS} = 50 V, f = 1 MHz)$	C <sub>oss</sub>		1 1	þr	
Common Source Feedback Capacitance			2.2		nF.
$(V_{GS} = 0V, V_{DS} = 50 V, f = 1 MHz)$	C <sub>RSS</sub>		2.2		pF

Load Mismatch (In Innogration Test Fixture, 50 ohm system): V<sub>DD</sub> = 50 Vdc, I<sub>DQ</sub> = 200 mA, f =108MHz, pulse width:100us, duty cycle:10%

Load 20:1 All phase angles, at 350W Pulsed CW Output Power	No Device Degradation
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# **MV0545VX LDMOS TRANSISTOR**

### TYPICAL CHARACTERISTICS

Figure 1: CW Gain and Power Efficiency as a Function of Pout at 30MHz

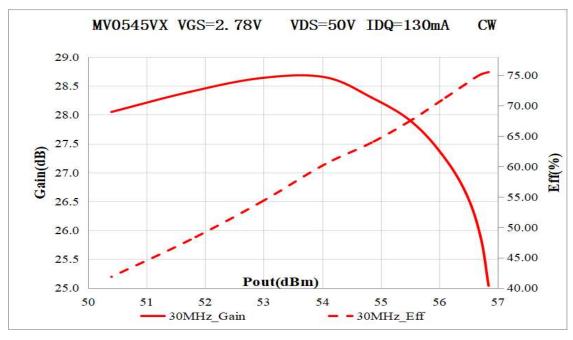


Figure 1: Network analyzer output S11/221



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# Reference Circuit of Test Fixture Assembly Diagram (PCB file upon request)

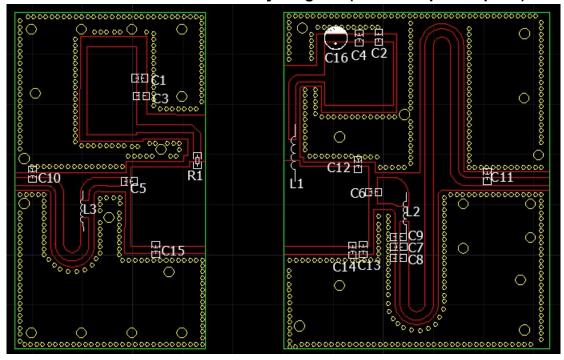


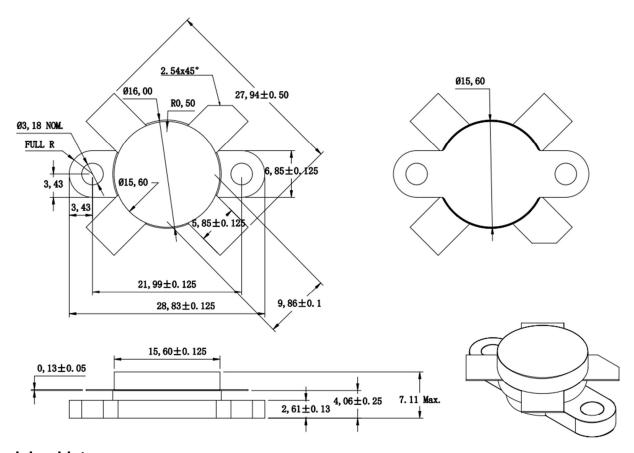
Table 1. Test Circuit Component Designations and Values (30MHz)

Component	Description	Suggested Manufacturer
C1,C2	10uF	10uF/100V
C3~C6	10nF	10nF/100V
C7	47pF	MQ101111
C8,C9,C14	100pF	MQ101111
C10	300pF	MQ101111
C11,C13	150pF	MQ101111
C12	56pF	MQ101111
C15	200pF	MQ101111
C16	4700uF/63V	Electrolytic Capacitor
R1	10 Ω	Chip Resistor
L1	d=1.5mm,D=5mm,19 Turns	
L2	d=1.5mm,D=5mm,5 Turns	
L3	d=1.5mm,D=5mm,7 Turns	
РСВ	30Mil	Rogers4350

# MV0545VX LDMOS TRANSISTOR

# **Package Outline**

Flanged ceramic package; 2 mounting holes; 2 leads (1—Gate, 2—Drain, 3—Source)



## **Revision history**

Table 5. Document revision history

Date	Revision	Datasheet Status
2023/12/4	Rev 1.0	Advanced datasheet generation
2024/3/25	Rev 1.0	Preliminary datasheet generation

Application data based on TC-24-16

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