



35W,50V Plastic RF LDMOS Transistor

ITGV22035C6

Description

The ITGV22035C6 is a dual path 35-watt, highly rugged, LDMOS transistor, designed for any general applications at frequencies 1.8 to 2.0GHz, in 10*6mm QFN plastic package, supporting surface mounted on PCB through high density grounding vias.

It can be configured as Doherty to be as high efficiency and low cost driver for 4G/5G application within 1.8 to 2.0GHz.



- Typical Doherty RF Performance (On Innogrator fixture with device soldered).

V_{ds}=50V I_{dq_main}=80mA, V_{gs_peak}=2.4V

Freq (MHz)	Pulse CW Signal			P _{avg} =32dBm WCDMA Signal		
	Gain P1dB (dB)	P3dB (W)	Eff@P3dB (%)	Gp (dB)	Eff(%)	ACPR _{5M} (dBc)
1805	15.19	41.55	43.49	15.55	21	-31.22
1842	15.55	39.46	44.58	16.63	23	-32.11
1880	14.57	45.36	47.58	15.71	21	-34.51

Features

- High Efficiency and Linear Gain Operations
- Integrated ESD Protection
- Excellent thermal stability, low HCI drift
- Large Positive and Negative Gate/Source Voltage Range for Improved Class C Operation
- Pb-free, RoHS-compliant

Suitable Applications

- L band power amplifier
- All 4G/5G cellular application within 1.8 to 2.0GHz

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V _{DSS}	+110	Vdc
Gate--Source Voltage	V _{GS}	-10 to +10	Vdc
Operating Voltage	V _{DD}	+55	Vdc
Storage Temperature Range	T _{stg}	-65 to +150	°C
Case Operating Temperature	T _c	+150	°C
Operating Junction Temperature	T _J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case T _c = 85°C, T _J =200°C, DC test	R _{θJC}	1.4	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22--A114)	Class 2

Table 4. Electrical Characteristics (TA = 25 °C unless otherwise noted)

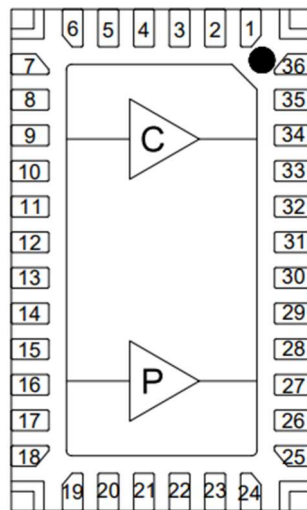
Characteristic	Symbol	Min	Typ	Max	Unit
DC Characteristics					
Drain-Source Voltage V _{GS} =0, I _{DS} =100uA	V _{(BR)DSS}		110		V
Zero Gate Voltage Drain Leakage Current (V _{DS} = 90V, V _{GS} = 0 V)	I _{DSS}	---	---	1	μA
Gate--Source Leakage Current (V _{GS} = 11 V, V _{DS} = 0 V)	I _{GSS}	---	---	1	μA
Gate Threshold Voltage (V _{DS} = 50V, I _D = 600 μA)	V _{GS(th)}	---	2	---	V
Gate Quiescent Voltage (V _{DD} = 50V, I _D = 80mA, Measured in Functional Test)	V _{GS(Q)}	---	3.6	---	V

Load Mismatch (In Innogrations Test Fixture, 50 ohm system): V_{DD} = 50Vdc, I_{DQ} = 80mA, f = 1800 MHz

VSWR 10:1 at 35W pulse CW Output Power	No Device Degradation
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Figure 1: Pin Connection definition

Transparent top view (Backside grounding for source)



Pin No.	Symbol	Description
8,9,10,11	RF IN/Vgs1	RF Input, Vgs bias for main path
14,15,16,17	RF IN/Vgs2	RF Input, Vgs bias for peak path
32,33,34,35	RF OUT/VDD1	RF Output, VDD bias for Main path
26,27,28,29	RF OUT/VDD2	RF Output, VDD bias for Peak path
Rest pins	NC	No connection
2,5,7,12,13,18,20,23,25,30,31,36, Package Base	GND	DC/RF Ground. Must be soldered directly to heatsink or copper coin for CW application.

**Reference Circuit of Test Fixture Assembly Diagram
20mils RO4350B**

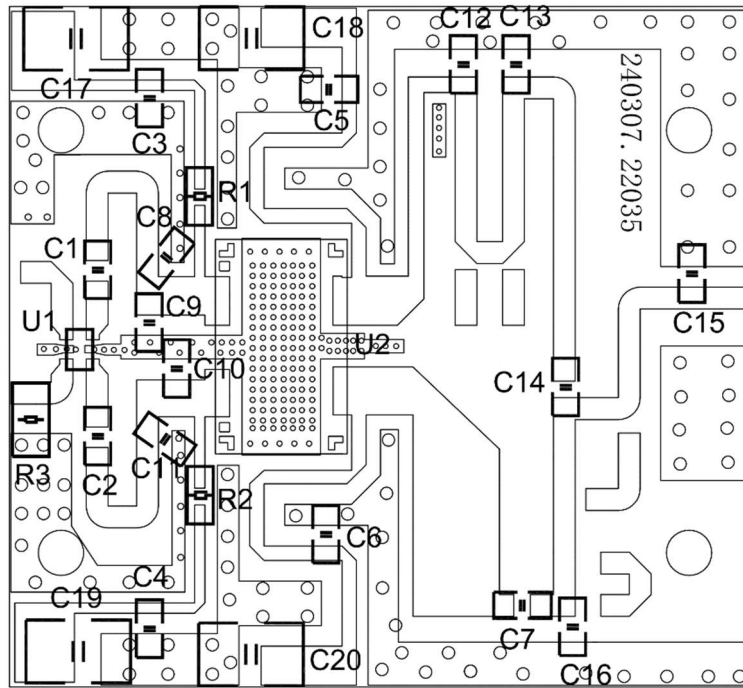


Figure 2. Test Circuit Component Layout

Table 5. Test Circuit Component Designations and Values

Reference	Footprint	Value	Quantity
C1, C2, C3, C4, C5, C6, C7	0603	20pF/250V	7
C8, C9, C10	0603	3.9pF/250V	3
C11	0603	3.6pF/250V	1
C12	0603	2.2pF/250V	1
C13	0603	0.2pF/250V	1
C16	0603	2.4pF/250V	1
C14	0603	15pF/250V	1
C15	0603	1.6pF/250V	1
C17, C18, C19, C20	1210	10uF/100V	4
R1, R2	0603	10R	2
R3	0805	51R	1
U1	0805	C1720J5003AHF	1
U2	C6	ITGV22035C6 ^{V1}	1



TYPICAL CHARACTERISTICS

Figure 5. Power Gain and Drain Efficiency as function of Power Output at Idq=80mA

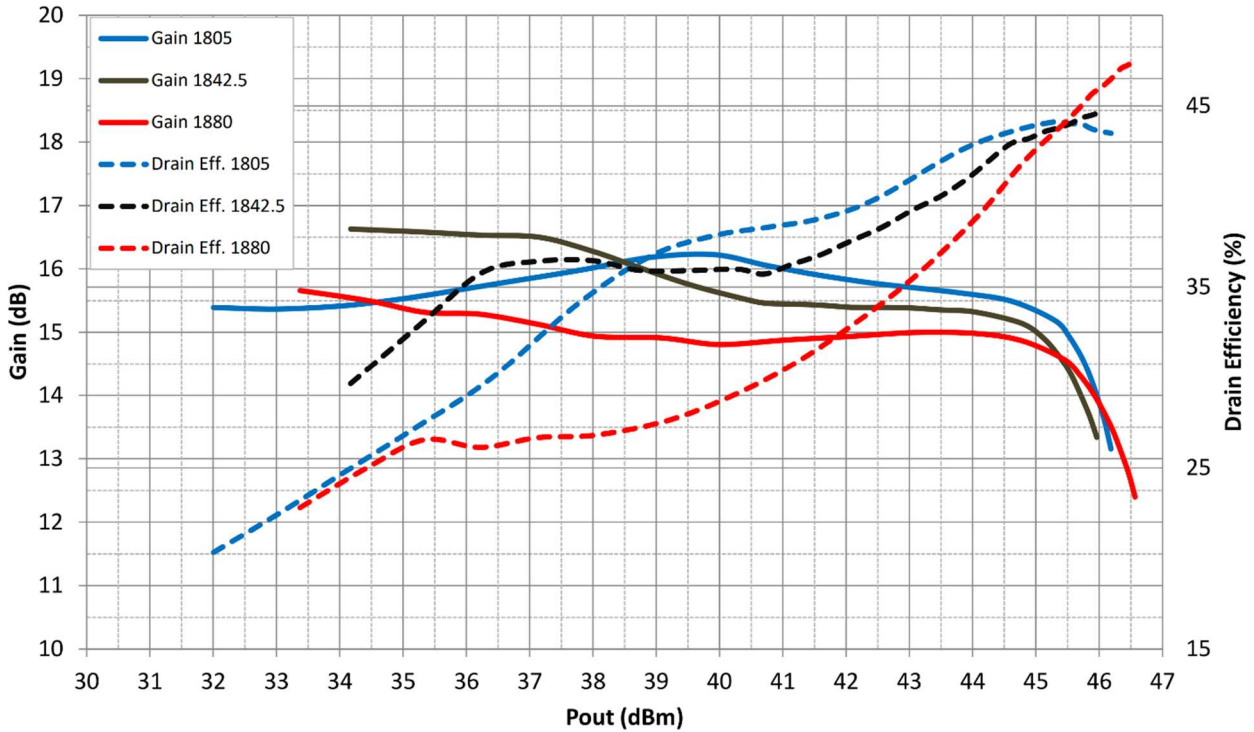
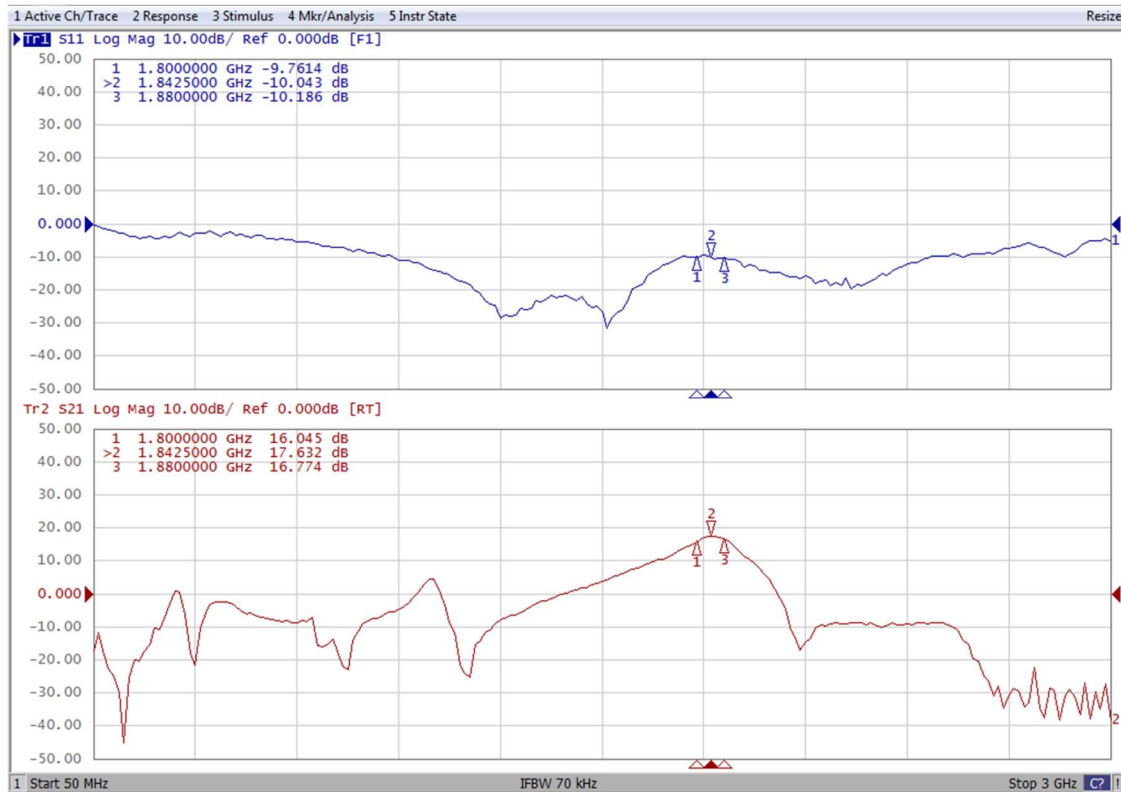


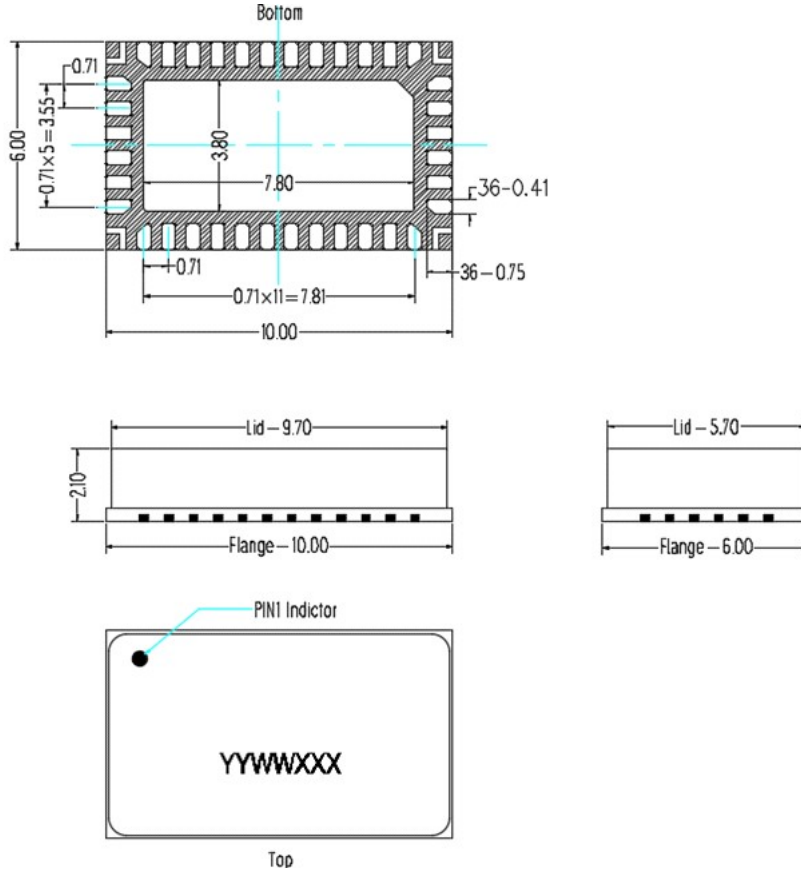
Figure 5. Network analyzer output S11/S21





Package Dimensions

10*6 Plastic Package



Notes:

1. All dimensions are in mm;
2. The tolerances unless specified are ±0.2mm.

Revision history

Table 7. Document revision history

Date	Revision	Datasheet Status
2024/4/9	Rev 1.0	Preliminary Datasheet

Application data based on ZBB-24-12

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