



## GaN 50V, 750W, 2.45GHz RF Power Transistor

**STCV25750D4**

### Description

The STCV25750D4 is a 750W capable, push pull, internally matched GaN HEMT, ideal for ISM or RF energy applications at 2450MHz narrow band

**In typical CW operation, it can deliver >700W CW when air cooling.**

There is no guarantee of performance when this part is used outside of stated frequencies.

- Typical RF performance at 2450MHz applications

Vds=50V, Vgs=-4.8V, CW, Tc=25 degree C, Air cooling, **heatsink size: 95\*130\*18mm**

Freq(MHz)	Pin(dBm)	Psat(dBm)	Psat(W)	IDS(A)	Gain(dB)	Eff(%)
2445	44.14	59.08	809.10	22.7	14.94	71.29
2450	44	58.99	792.50	22.26	14.99	71.20
2455	43.8	58.87	770.90	21.57	15.07	71.48

### Note:

**Performance might be varied under different load conditions due to loadpull effect, application report with isolator included upon request**

Recommended driver: STAV25050G2

### Applications

- 2.45GHz RF Energy
- S band power amplifier

### Important Note: Proper Biasing Sequence for GaN HEMT Transistors

#### Turning the device ON

1. Set VGS to the pinch--off (VP) voltage, typically -5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

#### Turning the device OFF

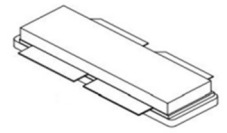
1. Turn RF power off
2. Reduce VGS down to VP, typically -5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain--Source Voltage	V <sub>DSS</sub>	+200	Vdc
Gate--Source Voltage	V <sub>GS</sub>	-8 to +0.5	Vdc
Operating Voltage	V <sub>DD</sub>	55	Vdc
Maximum gate current	I <sub>gs</sub>	102	mA
Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C
Case Operating Temperature	T <sub>C</sub>	+150	°C
Operating Junction Temperature	T <sub>J</sub>	+225	°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA T <sub>C</sub> = 25°C, at Pd=250W	R <sub>θJC</sub>	0.4	°C /W





**Table 3. Electrical Characteristics (TA = 25°C unless otherwise noted)**

**DC Characteristics (Each path, measured on wafer prior to packaging)**

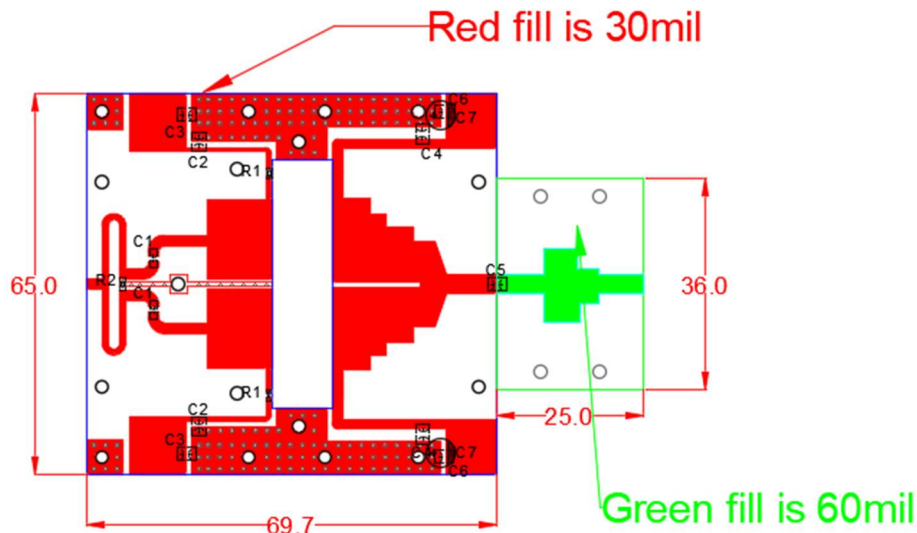
Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VGS=-8V; IDS=102mA	V <sub>DSS</sub>		200		V
Gate Threshold Voltage	VDS =10V, ID = 102mA	V <sub>GS(th)</sub>	-4	-	-2	V
Gate Quiescent Voltage	VDS =50V, IDS=120mA, Measured in Functional Test	V <sub>GS(Q)</sub>		-3.48		V

**Ruggedness Characteristics**

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	2.45GHz, Pout=750W pulse CW  All phase,  No device damages	VSWR		5:1		

**Reference Circuit of Test Fixture Assembly Diagram**

DXF file upon request

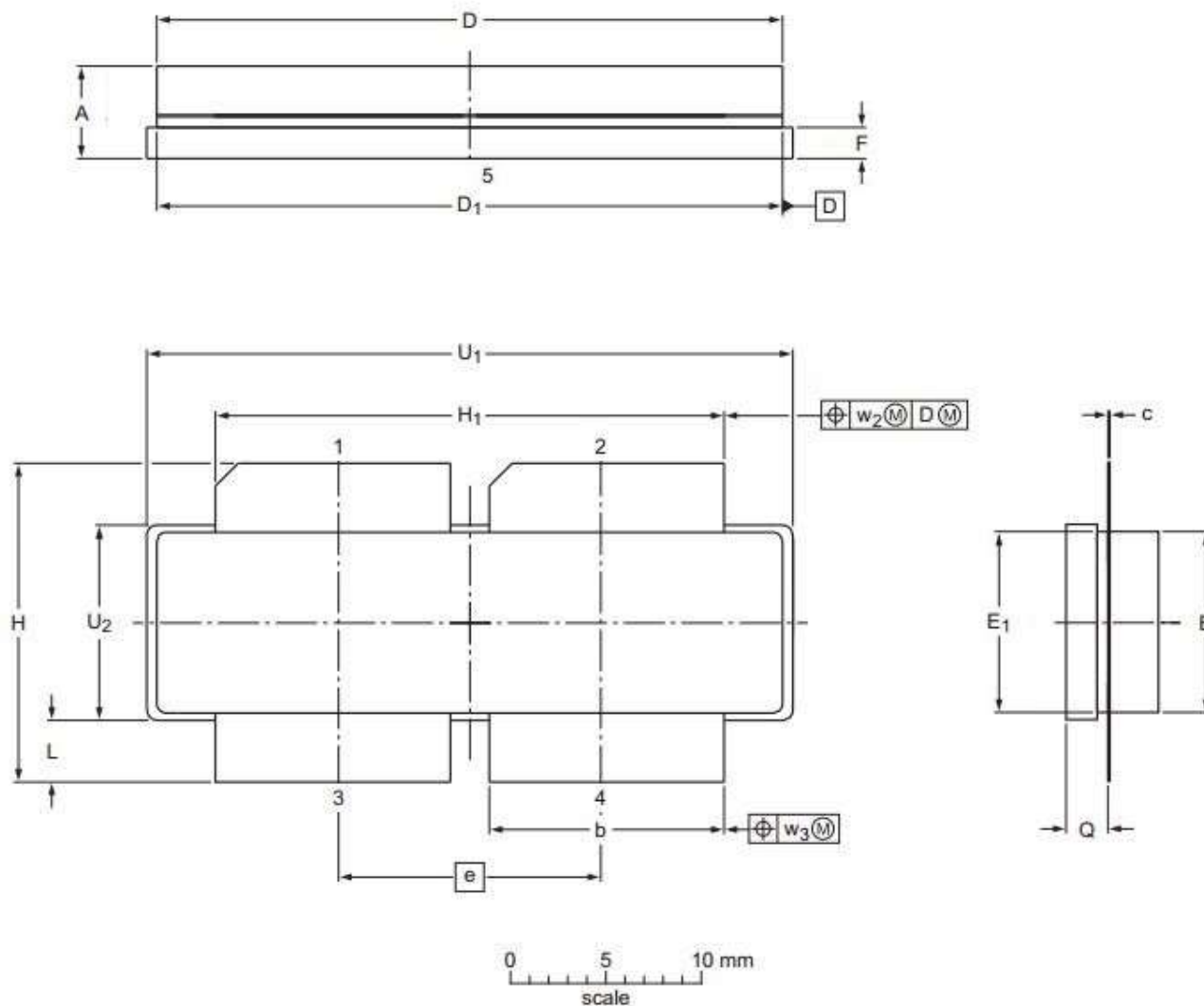


Component	Description	Suggestion
C1	18pF	MQ200805
C2	24pF	MQ301111
C4	15 pF	MQ301111
C5	MCM-1-300V-D-100-J	
C3,	10uF, 100V	1210
C6,	10uF, 100V	5750
C7	4700uF/63V	
R1	Chip Resistor, 10 $\Omega$	0805
R2	Chip Resistor, 100 $\Omega$	1206
PCB	Rogers tc350-plus, r= 3.5, thickness 30 mils, 1oz copper (red fill) ; //Taconic RF-35TC-0600-A, thickness 60 mils, 1oz copper(green fill)	



## Package Outline

Earless flanged ceramic package; 4 leads (1、2—DRAIN、3、4—GATE、5—SOURCE)



UNIT	A	b	c	D	D <sub>1</sub>	e	E	E <sub>1</sub>	F	H	H <sub>1</sub>	L	Q	U <sub>1</sub>	U <sub>2</sub>	W <sub>2</sub>	W <sub>2</sub>
mm	4.7	11.81	0.18	31.55	31.52	13.72	9.50	9.53	1.75	17.12	25.53	3.48	2.26	32.39	10.29	0.25	0.25
	4.2	11.56	0.10	30.94	30.96		9.30	9.27	1.50	16.10	25.27	2.97	2.01	32.13	10.03		
inches	0.185	0.465	0.007	1.242	1.241	0.540	0.374	0.375	0.069	0.674	1.005	0.137	0.089	1.275	0.405	0.01	0.01
	0.165	0.455	0.004	1.218	1.219		0.366	0.365	0.059	0.634	0.995	0.117	0.079	1.265	0.395		

OUTLINE VERSION	REFERENCE			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
PKG-D4					03/12/2013



## Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2023/6/7	Rev 1.0	Preliminary datasheet creation
2024/7/25	Rev 1.1	Update application result based on enlarged heatsink

Application data based on: YHG-23-11/24-10

## Notice

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