



GaN HEMT 50V, 280W, 0.6-1.0GHz RF Power Transistor

Description

The STBV10280C9 is a 280watt capable Doherty pair, GaN HEMT, ideal for 4G/5G cellular applications from 0.6 to 1GHz..

It can be configured as asymmetrical Doherty delivering 30-40W average power, according to normal 8.5-9.5dB back off.

There is no guarantee of performance when this part is used outside of stated frequencies.

- Typical RF performance on **758-803MHz** full band asymmetrical Doherty with device soldered
VDS= 50V, IDQ=100mA(Vgm=-3.22V, Vgp=-5.8V)

STBV10280C9



ACPR @46.5dBm_1C-WCDMA

Freq (MHz)	ACPR (dBc)	Gain (dB)	Efficiency (%)
758	-28.11	17.25	62.32
780	-28.85	17.06	61.45
803	-29.52	16.75	62.24

(1)1C WCDMA; Signal PAR = 10 dB @ 0.01% Probability on CCDF.

- Typical RF performance on **859-894MHz** full band asymmetrical Doherty with device soldered
VDS= 50V, IDQ=60mA(Vgm=-3.25V, Vgp=-5V)

Freq (MHz)	Pout (dBm)	CCDF (dB)	Ppeak (dBm)	Ppeak (W)	ACPR (dBc)	Gain (dB)	Efficiency (%)
859	46.56	7.92	54.48	280.6	-31.1	18.9	62.1
876	46.58	8.17	54.75	298.5	-30.7	18.7	62.8
894	46.59	8.10	54.69	294.3	-29.6	18.5	62.6

(1)1C WCDMA; Signal PAR = 10 dB @ 0.01% Probability on CCDF.

Applications

- Asymmetrical Doherty amplifier within 0.6-1GHz
- UHF TV
- P band power amplifier

Important Note: Proper Biasing Sequence for GaN HEMT Transistors

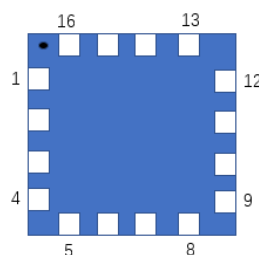
Turning the device ON

- Set VGS to the pinch--off (VP) voltage, typically -5 V
- Turn on VDS to nominal supply voltage
- Increase VGS until IDS current is attained
- Apply RF input power to desired level

Turning the device OFF

- Turn RF power off
- Reduce VGS down to VP, typically -5 V
- Reduce VDS down to 0 V
- Turn off VGS

Pin Configuration and Description (Top view)





Pin No.	Symbol	Description
1,2	RF IN/Vgs of Main	RF Input/Gate bias of main path
3,4	RF IN/Vgs of Peak	RF Input/Gate bias of peak path
9,10	RF OUT/Vds of Peak	RF Output/Drain bias of peak path
11,12	RF OUT/Vds of Main	RF Output/Drain bias of main path
Other Pins	GND	Grounding
Package Base	GND	DC/RF Ground. Proposed to be soldered to heatsink plane directly for the best CW thermal and RF performance. Soldered through vias or copper coin allowed for pulsed CW and back off applications, but will result in higher junction temperatures

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	V_{DSS}	+200	Vdc
Gate--Source Voltage	V_{GS}	-8 to +0.5	Vdc
Operating Voltage	V_{DD}	55	Vdc
Maximum gate current	I_{gs}	33.6	mA
Storage Temperature Range	T_{stg}	-65 to +150	°C
Case Operating Temperature	T_C	+150	°C
Operating Junction Temperature	T_J	+225	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA $T_C = 85^\circ\text{C}$, at $P_d = 30\text{W}$, on Doherty application board	$R_{\theta JC}$	3	°C /W

Table 3. Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise noted)

DC Characteristics (Main path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = -8\text{V}$; $I_{DS} = 16.8\text{mA}$	V_{DSS}		200		V
Gate Threshold Voltage	$V_{DS} = 10\text{V}$, $I_D = 16.8\text{mA}$	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	$V_{DS} = 50\text{V}$, $I_{DS} = 100\text{mA}$, Measured in Functional Test	$V_{GS(Q)}$		-3.2		V

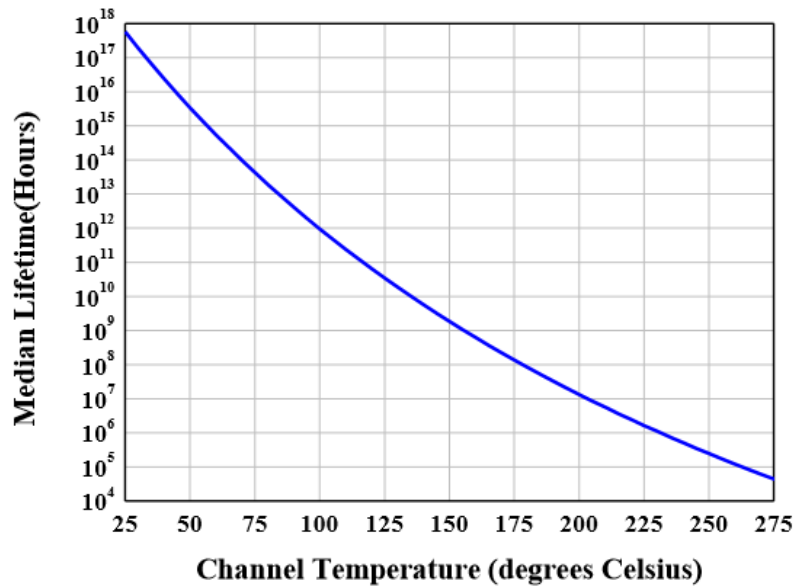
DC Characteristics (Peak path, measured on wafer prior to packaging)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = -8\text{V}$; $I_{DS} = 16.8\text{mA}$	V_{DSS}		200		V
Gate Threshold Voltage	$V_{DS} = 10\text{V}$, $I_D = 16.8\text{mA}$	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	$V_{DS} = 50\text{V}$, $I_{DS} = 100\text{mA}$, Measured in Functional Test	$V_{GS(Q)}$		-3.2		V

Ruggedness Characteristics

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	1GHz, $P_{out} = 45\text{W}$ WCDMA 1 Carrier in Doherty circuit All phase, No device damages	VSWR		10:1		

Figure 2: Median Lifetime vs. Channel Temperature



758-803MHz

Figure 3: Efficiency and power gain as function of Pout

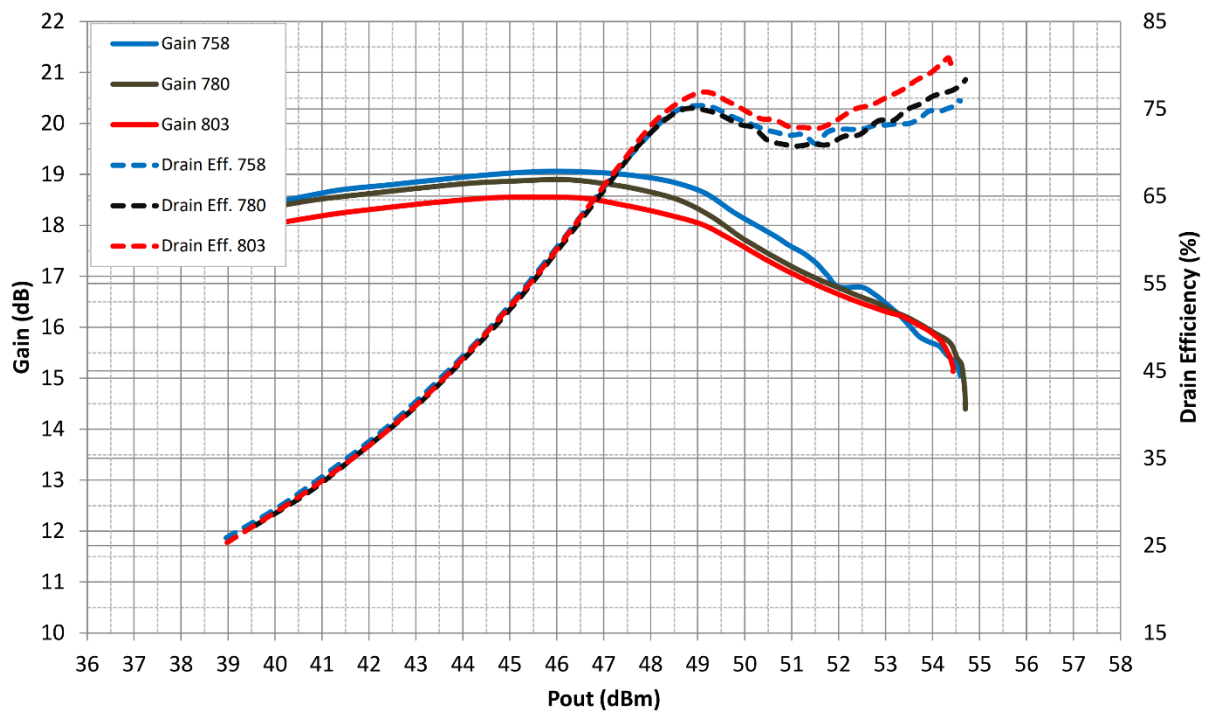


Figure 4: Network analyzer output, S11 and S21

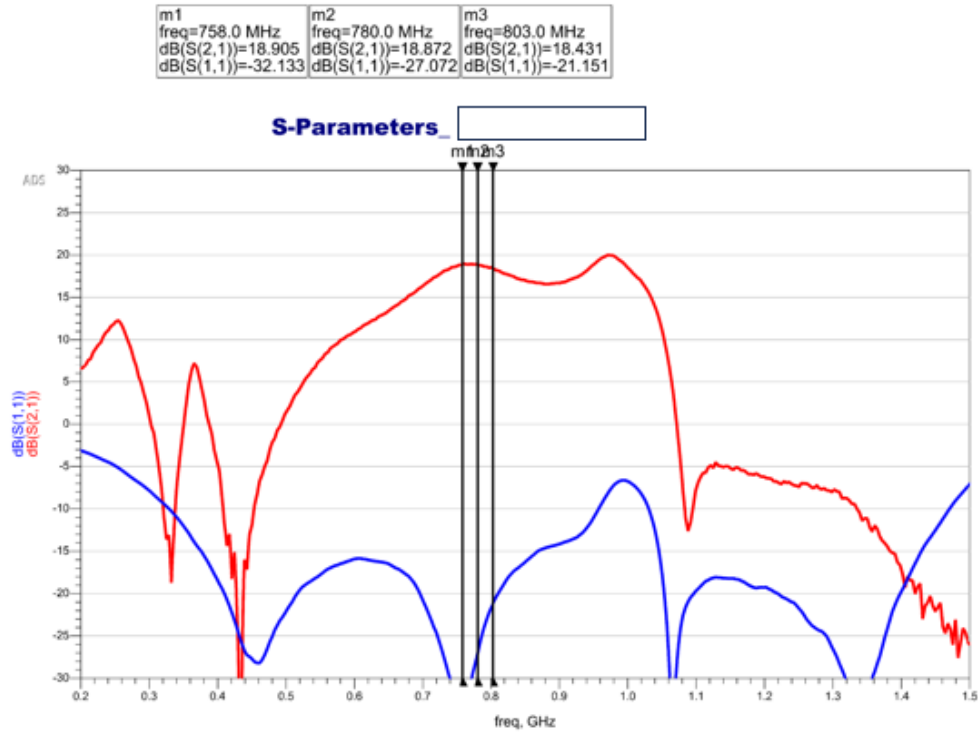


Figure 5: Picture of application board Doherty circuit

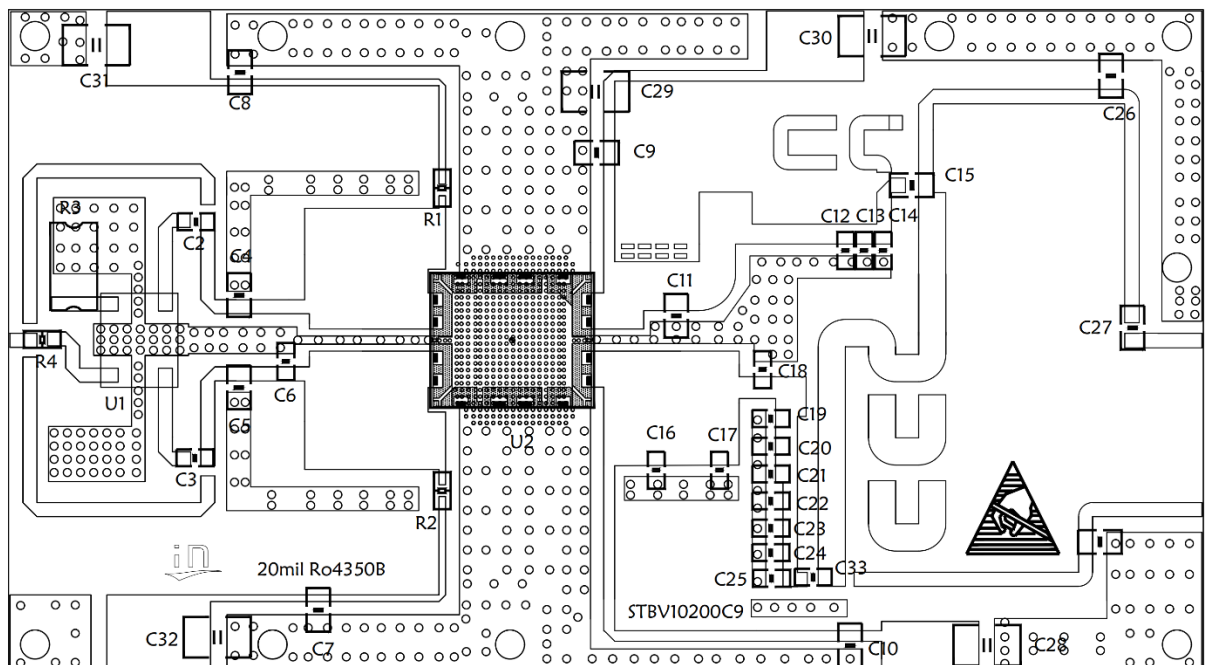




Table 4. Bill of materials of application board (PCB layout upon request, RO4350B 20mils)

Reference	Footprint	Value	Quantity
C2, C3, C7, C8, C9, C10, C15, C27, C33	0603	100pF/250V	9
C4, C5	0603	10pF/250V	2
C6, C20, C22	0603	1.1pF/250V	3
C11	0603	6.8pF/250V	1
C12, C13, C14, C18, C25	0603	2.4pF/250V	5
C16	0603	5.6pF/250V	1
C17	0603	0.3pF/250V	1
C19	0603	1.8pF/250V	1
C21	0603	2.0pF/250V	1
C23	0603	3.9pF/250V	1
C24	0603	0.2pF/250V	1
C26	0603	3.3pF/250V	1
C28, C29, C30, C31, C32	1210	10uF/100V	5
R1, R2	0603	10R	2
R3	2512	51R	1
U1	3.18*5.08mm	X3C07F1-02S	1
U2	C9	STBV10280C9	1

859-894MHz

Figure 6: Efficiency and power gain as function of Pout

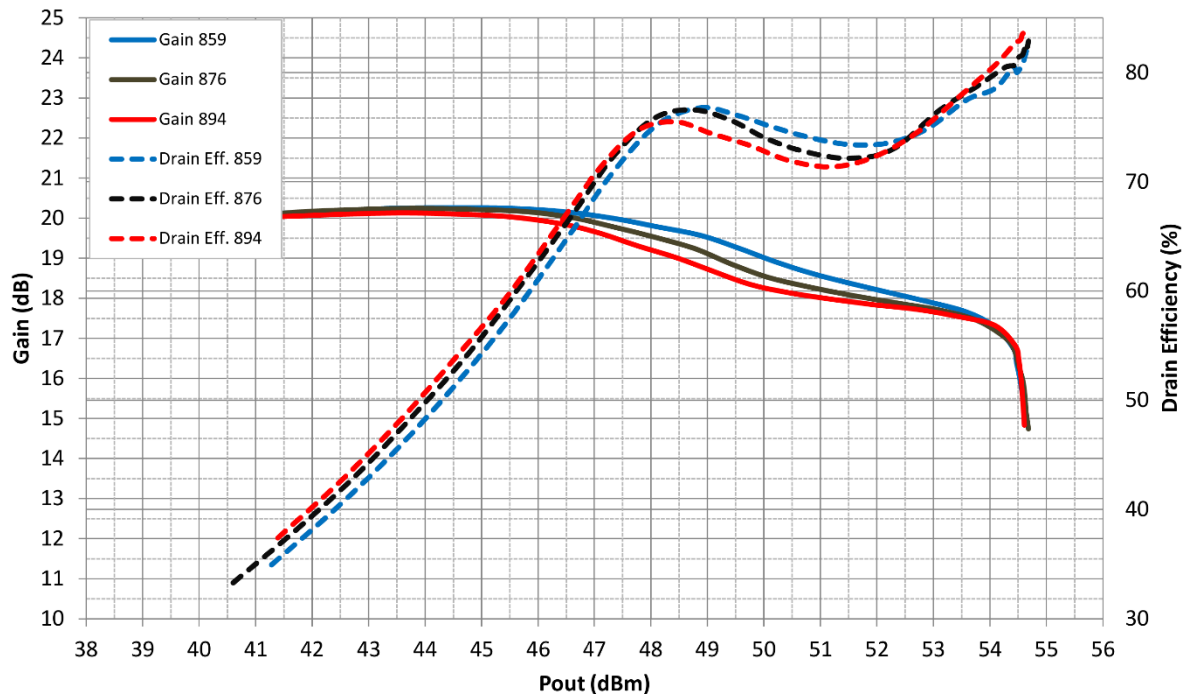




Figure 7: Network analyzer output, S11 and S21

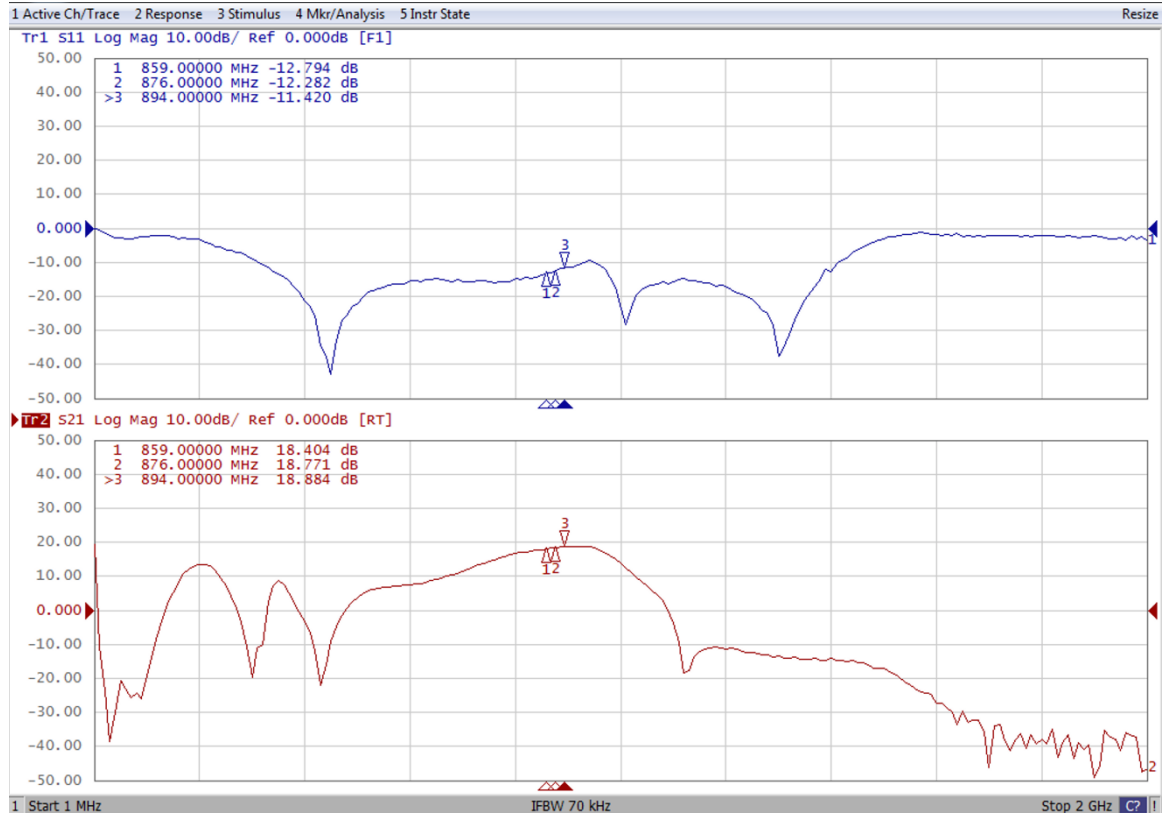


Figure 8: Picture of application board Doherty circuit

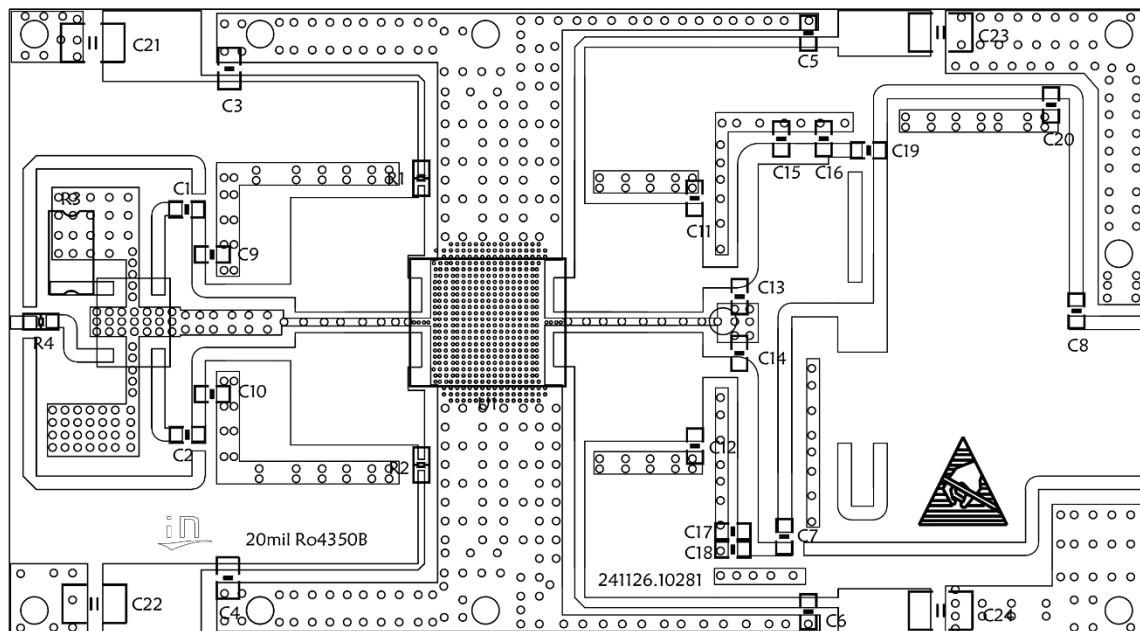


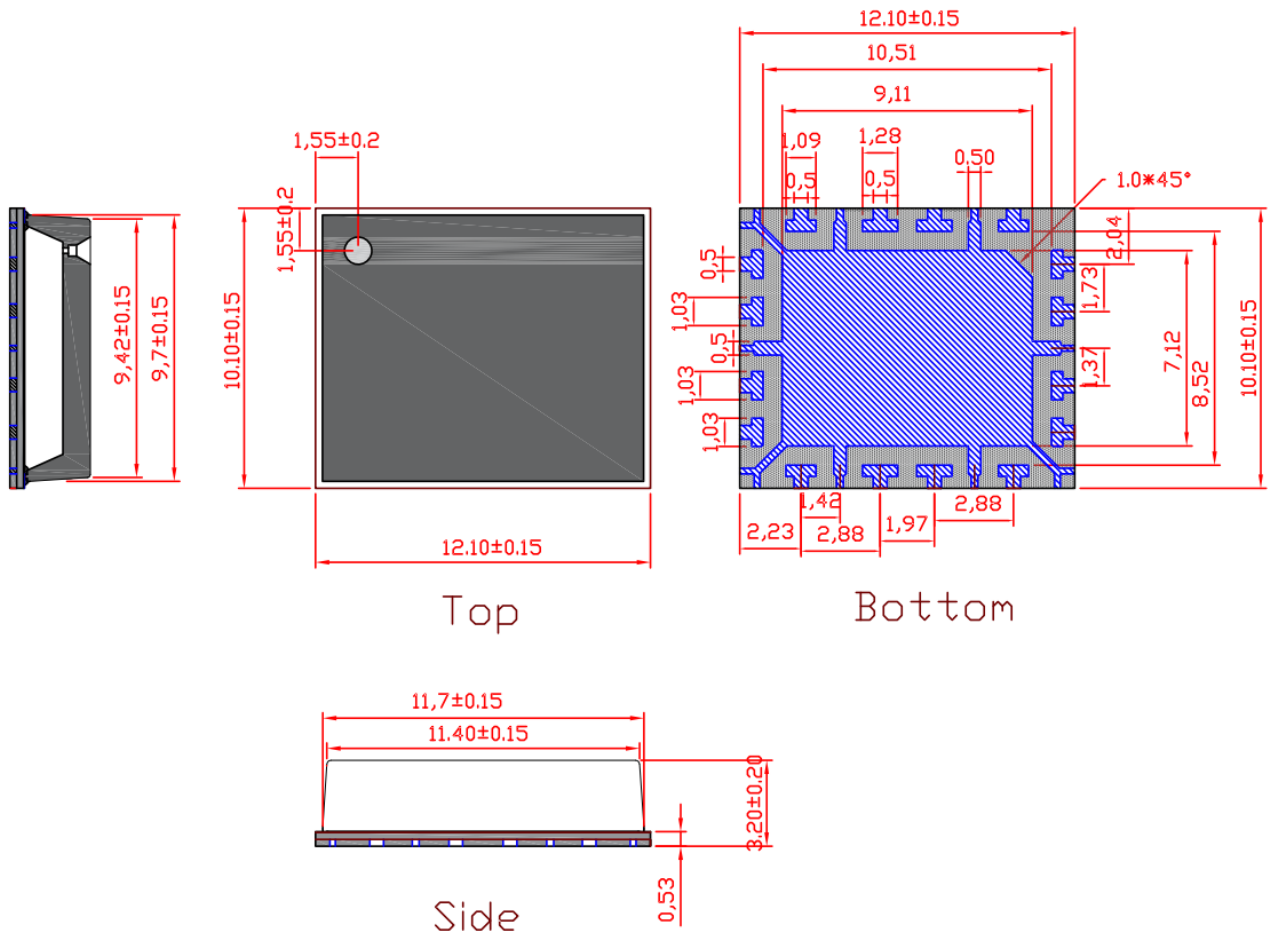


Table 5. Bill of materials of application board (PCB layout upon request, RO4350B 20mils)

Reference	Footprint	Value	Quantity
C1, C2, C3, C4, C5, C6, C7, C8	0603	68pF/250V	8
C9, C10	0603	6.8pF/250V	2
C14	0603	1.0pF/250V	1
C11, C12, C13, C14, C15, C16, C17	0603	2.0pF/250V	7
C18	0603	3.3pF/250V	1
C19	0603	10pF/250V	1
C20	0603	3.0pF/250V	1
C21, C22, C23, C24	1210	10uF/100V	4
R1, R2	0603	10R	2
R3	2512	51R	1
R4	0603	0R	1
U2	3.18*5.08mm	DC07F02	1
U1	C9	STBV10280C9 ^{V3}	1



Package Dimensions (Unit:mm)



Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2023/6/25	V1.0	Preliminary Datasheet Creation
2023/8/17	V1.1	Modification of package drawing on last page
2024/11/26	V1.2	Add 859-894M,728-768M new application result

Application data based on: ZBB-23-20/24-51/24-52

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