



## DC-0.5GHz, 2W, 50V LDMOS Fully matched PA Module

### Description

The IMGV0005-2 is a 2-watt ,single stage integrated Power Amplifier Module, designed for broad band applications, with frequencies from DC to 0.5GHz. The module is 50  $\Omega$  input/output matched and requires minimal external components.

The module implements distributed power amplifier in form of multi chips, housed in cost effective plastic open cavity package, offers a much lower cost than traditional MMIC solutions.

V<sub>ds</sub>=50V, I<sub>dq</sub>=20mA, CW

Parameter	30MHz	100MHz	200MHz	300MHz	400MHz	500MHz	600MHz	Units
Linear Gain	11.3	11.3	11.3	11.3	11.1	11.1	10.6	dB
Gain@Pin=24dBm	8.5	8.8	8.9	8.9	8.8	8.7	8.4	dB
Pout@Pin=24dBm	1.8	1.9	1.9	2.0	1.9	1.9	1.7	W
Gain@P3dB	8.3	8.3	8.3	8.3	8.1	8.1	7.6	dB
Pout@P3dB	1.8	2.0	2.0	2.1	2.0	2.0	1.8	W



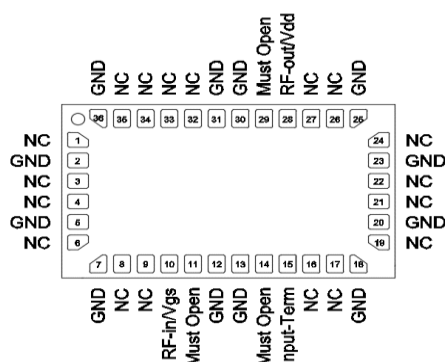
### Product Features

- Operating Frequency Range: DC-0.5GHz
- Operating Drain Voltage: +50 V
- 50  $\Omega$  Input/Output
- Psat: 2W
- Small signal gain:>11dB, Power gain:>8dB
- 6x10 mm Surface Mount Package
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC
- Much lower cost than GaN-based ultrawide band PA , due to LDMOS technology used

### Applications

- Ultra Broadband Amplifiers
- Driver for ISM, FM
- Test Instrumentation
- EMC Amplifier Drivers
- HF/VHF 2-way Radios

### Pin Configuration and Description





Top View

Pin No.	Symbol	Description
28	RFout/Vdd	Transistor 1, Drain Bias & RF Output
10	RFin/Vgs	Transistor 1, RF Input & Gate Bias
15	Input-Term	Transistor 1, Input 50 ohm term
Others	NC	No connection
11, 14, 29	Must Open	Keep the pin open, no GND
2,5,7,12,13,16,20,23,25, 30, 31,36 Package Base	GND	DC/RF Ground. Must be soldered to EVB ground plane over array of vias for thermal and RF performance. Solder voids under Pkg Base will result in excessive junction temperatures causing permanent damage.

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain--Source Voltage	$V_{DS}$	115	Vdc
Gate--Source Voltage	$V_{GS}$	-10 to +10	Vdc
Operating Voltage	$V_{DD}$	+50	Vdc
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature	$T_c$	+150	°C
Operating Junction Temperature	$T_J$	+200	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case $T_C = 25^{\circ}\text{C}$ , DC test	$R_{\theta JC}$	15	°C/W

Table 3. Electrical Characteristics

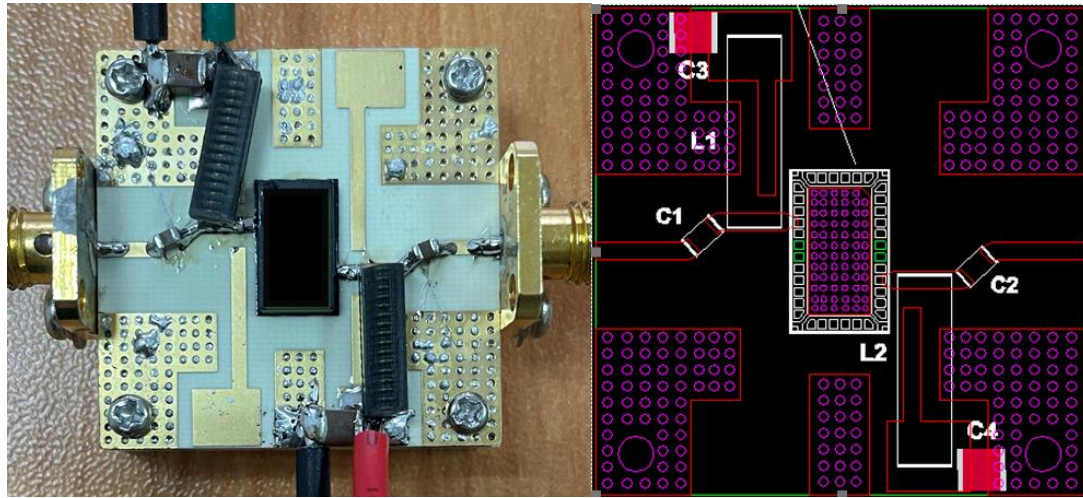
Parameter	Condition	Min	Typ	Max	Unit
Frequency Range	Pin=24dBm	30		500	MHz
Power Gain @ Psat	Pin=24dBm	8			dB
$P_{SAT}$	Pin=24dBm		33		dBm
Drain Efficiency @ $P_{SAT}$	Pin=24dBm		20		%

Unless otherwise noted:  $T_A = 25^{\circ}\text{C}$ ,  $V_{DD} = 50\text{ V}$ , Pulse Width=100 us, Duty cycle=10%Load Mismatch of per Section (On Test Fixture, 50 ohm system):  $V_{DD} = 50\text{ V}$ ,  $I_{DQ} = 20\text{ mA}$ ,  $f = 0.5\text{GHz}$ 

SWR 10:1 at Psat pulse CW Output Power	No Device Degradation
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## Reference Circuit of Test Fixture Assembly Diagram



		Part NO.	Vendor
C3,C4	10uF 100V Chip Capacitor	C5750X7S2A106M230KB	TDK
C1,C2	50V 1uF Chip Capacitor	GRM21BR71H105KA12L	muRata
L1,L2	1.3uH 4.2A Inductor	4310LC-132KEC	Coilcraft
PCB	RO4350B,20mil,er=3.48		

## TYPICAL CHARACTERISTICS

Figure 1. Network analyzer output S11/S21 (Pin=0dBm)

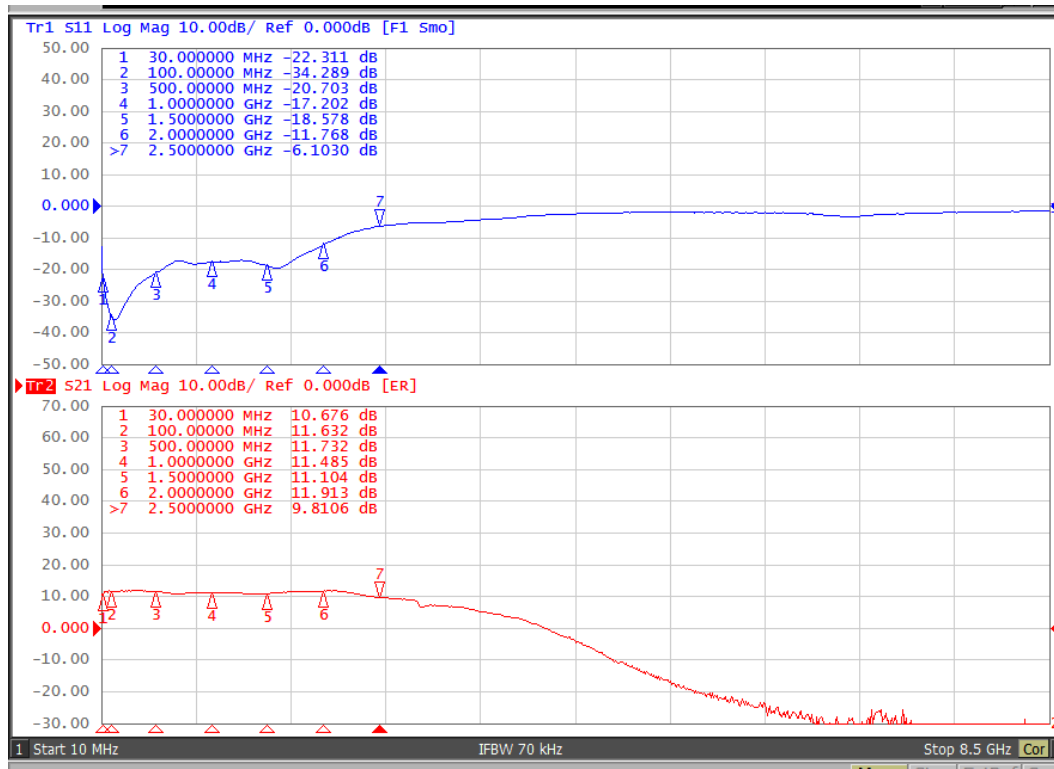
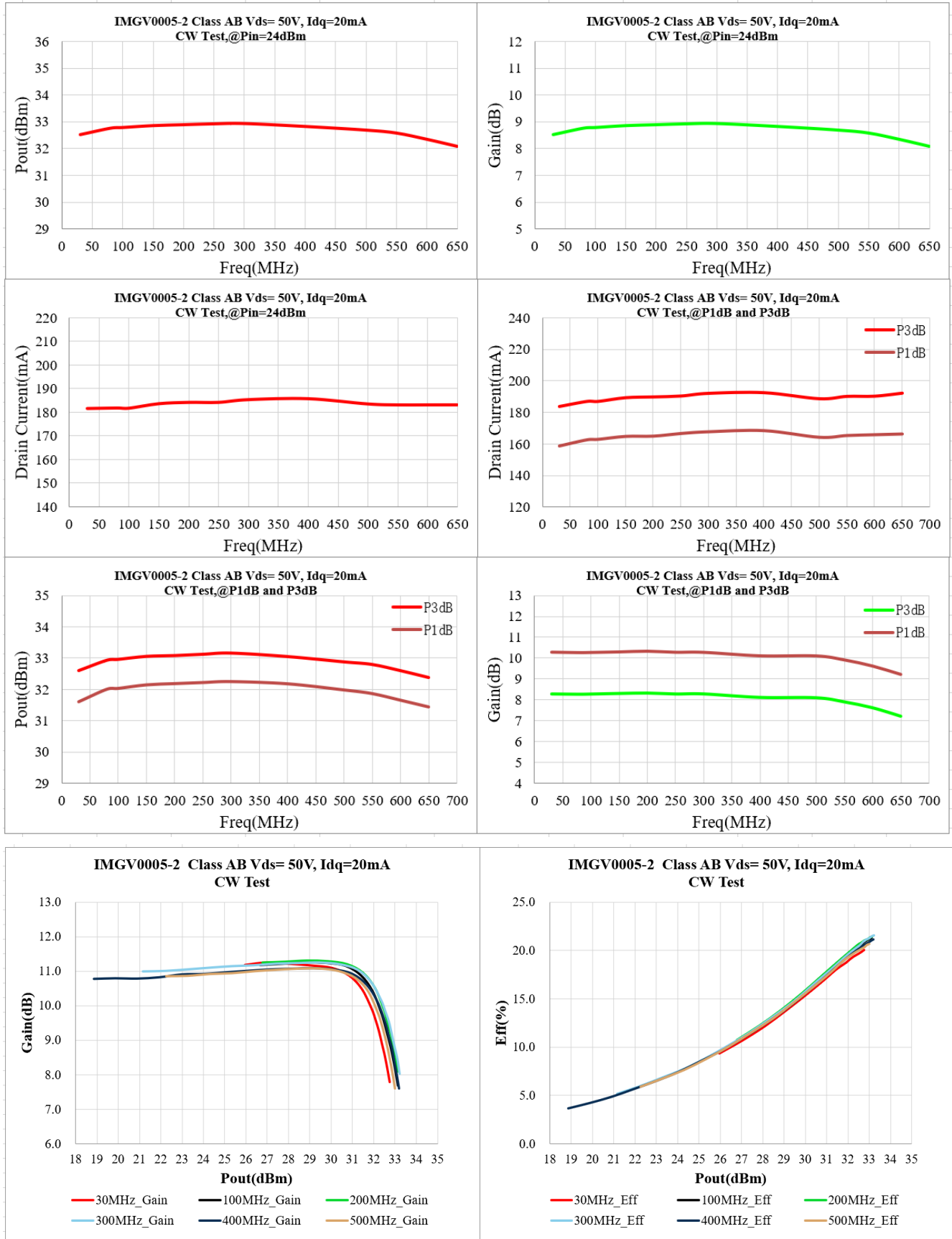


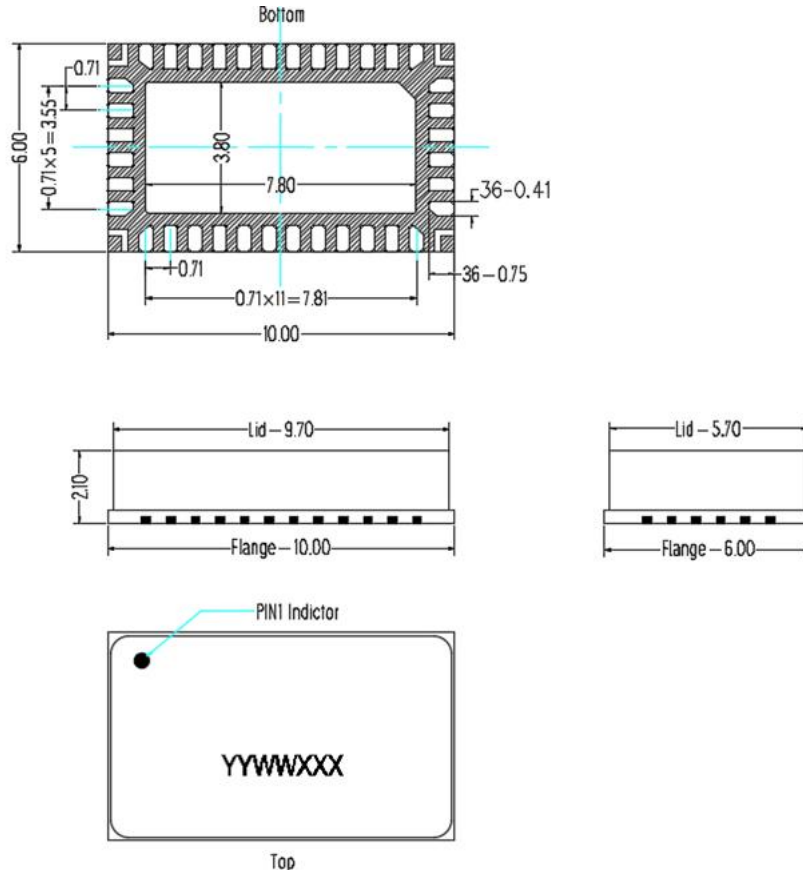


Figure. Power Gain and, efficiency and Pout @Pin=24dBm ,and P1dB,P3dB vs. Frequency



## Package Dimensions

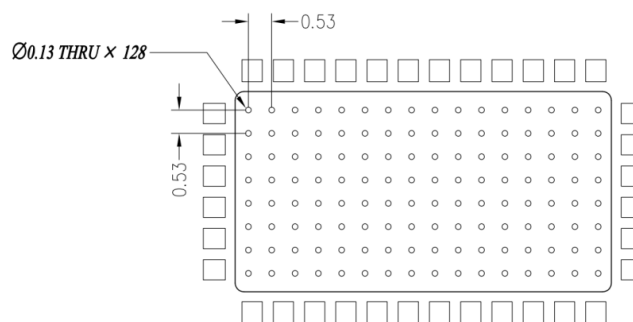
### 10\*6 Plastic Package



#### Notes:

1. All dimensions are in mm;
2. The tolerances unless specified are  $\pm 0.2$ mm.

## Mounting Footprint Pattern



#### Notes:

1. All dimensions are in mm;
2. Vias are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. ALL vias are PTH to ground.



## Revision history

Table 6. Document revision history

Date	Revision	Datasheet Status
2024/10/17	Rev 1.0	Production Datasheet

Application data based on ZHH-24-10

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