



## GaN HEMT 50V, 140W, 1.8-2.7GHz Power Transistor

**STAV27140C6**

### Description

The STAV27140C6 is a dual path 140W, internal matched GaN HEMT, operated from 1.8-2.7GHz. It features high gain, high efficiency, wide band and low cost, in 10\*6mm open cavity plastic package. It can be configured as a single stage asymmetrical Doherty capable of delivering  $P_{avg}$  of 20W. There is no guarantee of performance when this part is used outside of stated frequencies.

➤ Typical Doherty Single--Carrier W--CDMA Characterization Performance at 1.8GHz:

Input Signal :WCDMA 1 Carrier with PAR = 10 dB @ 0.01% Probability on CCDF , Pulsed CW: 20us, 10%

$V_{DD} = 50$  Vdc,  $I_{DQA} = 60$ mA,  $V_{GSB} = -5.5$ Vdc,



Freq (MHz)	Pulse CW Signal			Pavg=43dBm WCDMA Signal		
	P1-Gain (dB)	Psat (dBm)	Psat (W)	Gp (dB)	Eff (%)	ACPR5M (dBc)
1805	15.22	51.60	144.43	15.70	58.80	-29.85
1842.5	15.28	51.62	145.23	15.66	59.42	-30.69
1880	15.21	51.54	142.56	15.57	59.38	-32.59

### Applications

- 5G Doherty amplifier within 2.5-2.7, 2.1-2.2, 1.8-1.9G either as driver or as final
- S band power amplifier
- L band power amplifier

### Important Note: Proper Biasing Sequence for GaN HEMT Transistors

#### Turning the device ON

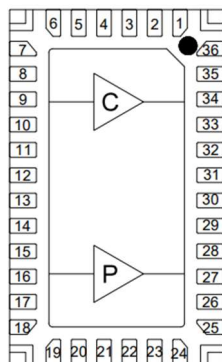
1. Set VGS to the pinch--off (VP) voltage, typically -5 V
2. Turn on VDS to nominal supply voltage
3. Increase VGS until IDS current is attained
4. Apply RF input power to desired level

#### Turning the device OFF

1. Turn RF power off
2. Reduce VGS down to VP, typically -5 V
3. Reduce VDS down to 0 V
4. Turn off VGS

Figure 1: Pin Connection definition

Transparent top view (Backside grounding for source)



Pin No.	Symbol	Description
9,10	RF IN/Vgs1	RF Input, Vgs bias for main path



15,16	RF IN/Vgs2	RF Input, Vgs bias for peak path
33,34	RF OUT/VDD1	RF Output, VDD bias for Main path
27,28	RF OUT/VDD2	RF Output, VDD bias for Peak path
Rest pins	NC	No connection
2,5,7,12,13,18,20,23,25,30,31,36, Package Base	GND	DC/RF Ground. Must be soldered directly to heatsink or copper coin for CW application.

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain--Source Voltage	$V_{DS}$	+200	Vdc
Gate--Source Voltage	$V_{GS}$	-8 to +0.5	Vdc
Operating Voltage	$V_{DD}$	55	Vdc
Maximum gate current	$I_{GS}$	17.5	mA
Storage Temperature Range	$T_{stg}$	-65 to +150	°C
Case Operating Temperature	$T_C$	+150	°C
Operating Junction Temperature	$T_J$	+225	°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case by FEA $T_C = 85^\circ\text{C}$ , $P_{diss} = 15\text{W}$ at $P_{avg} = 43\text{dBm}$ WCDMA 1 carrier	$R_{\theta JC}$	2.2	°C /W

Notes: Based on expected carrier amplifier efficiency of Doherty,  $P_{avg}$  assumes 10% peaking amplifier contribution of total average Doherty rated power. Thermal resistance is measured to package backside

**Table 3. Electrical Characteristics ( $T_A = 25^\circ\text{C}$  unless otherwise noted)**

**DC Characteristics (main path, measured on wafer prior to packaging)**

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = -8\text{V}$ ; $I_{DS} = 7.5\text{mA}$	$V_{DSS}$		200		V
Gate Threshold Voltage	$V_{DS} = 10\text{V}$ , $I_D = 7.5\text{mA}$	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	$V_{DS} = 50\text{V}$ , $I_{DS} = 60\text{mA}$ , Measured in Functional Test	$V_{GS(Q)}$		-3.1		V

**DC Characteristics (peak path, measured on wafer prior to packaging)**

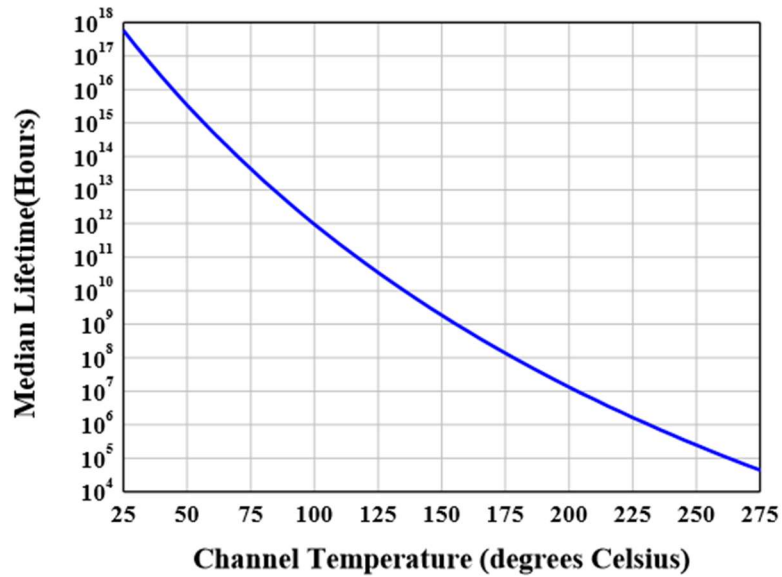
Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	$V_{GS} = -8\text{V}$ ; $I_{DS} = 10\text{mA}$	$V_{DSS}$		200		V
Gate Threshold Voltage	$V_{DS} = 10\text{V}$ , $I_D = 10\text{mA}$	$V_{GS(th)}$	-4		-2	V
Gate Quiescent Voltage	$V_{DS} = 50\text{V}$ , $I_{DS} = 90\text{mA}$ , Measured in Functional Test	$V_{GS(Q)}$		-3.1		V

**Ruggedness Characteristics**

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Load mismatch capability	2.6GHz, $P_{out} = 43\text{dBm}$ WCDMA 1 Carrier, All phase, No device damages	VSWR		10:1		



Figure 2: Median Lifetime vs. Channel Temperature



**Typical performance**  
**1805-1880MHz Doherty**

Figure 3: Efficiency and power gain as function of Pout

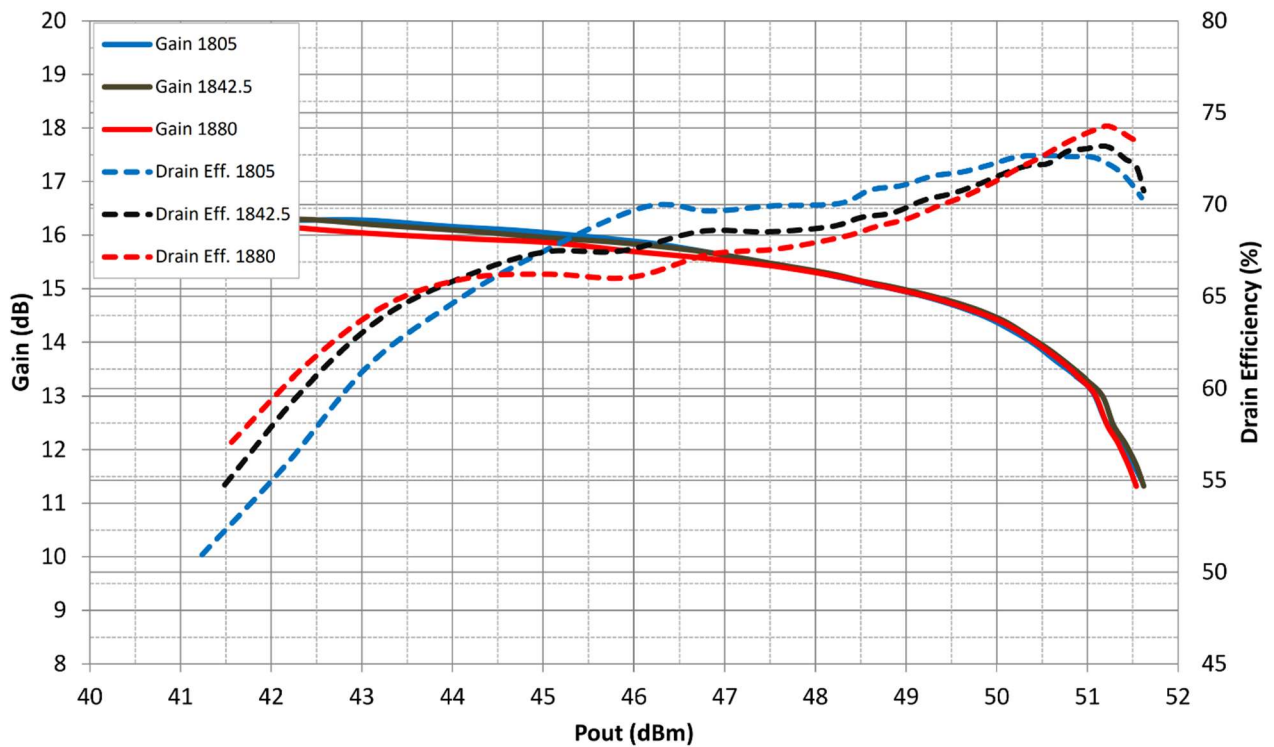




Figure 4: Network analyzer output, S11 and S21

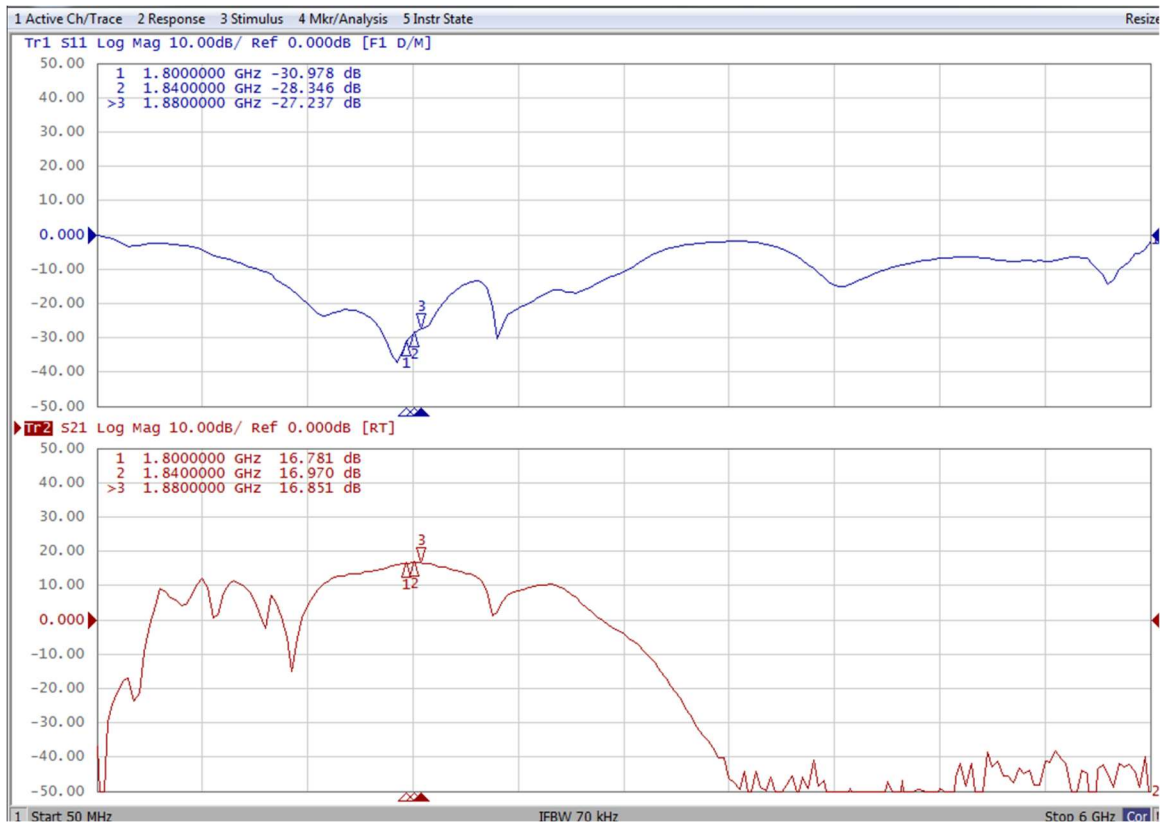
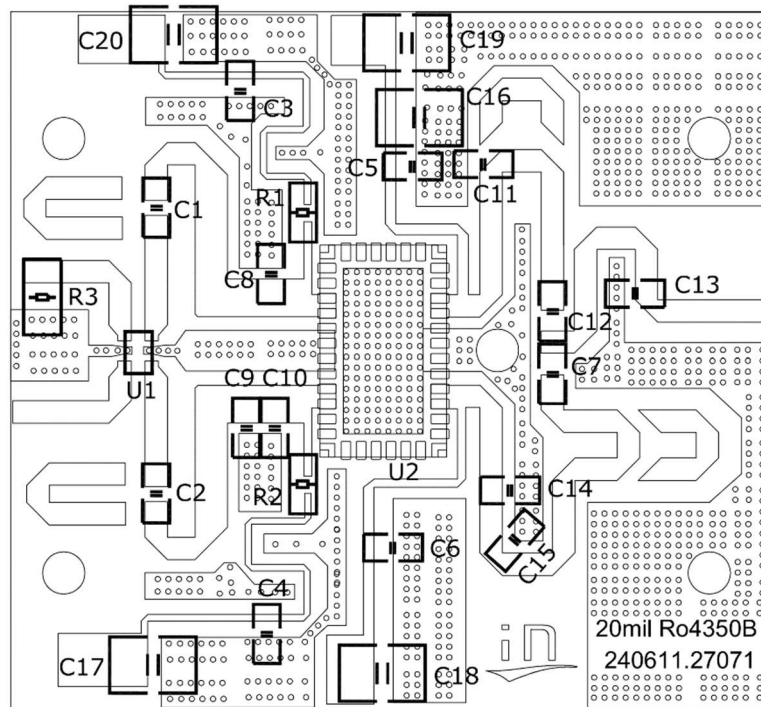


Figure 5: Picture of application board Doherty circuit

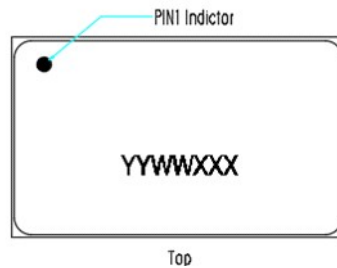
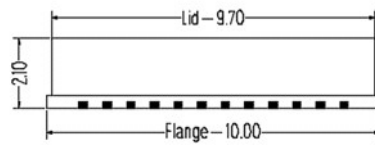
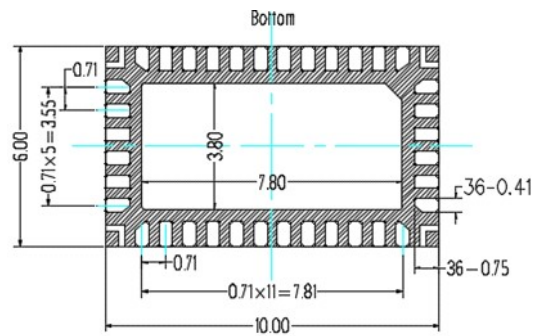




**Table 4. Bill of materials of application board (PCB layout upon request, RO4350B 20mils)**

Component	Value	Quantity
U1	C1720J5003AHF	1
U2	STAV27140C6	1
C1	8.2pF/250V	1
C8, C10	2.7pF/250V	2
C9	0.5pF/250V	1
C11, C15	2.0pF/250V	2
C14	0.9pF/250V	1
C12	4.3pF/250V	1
C13	1.3pF/250V	1
C2, C3, C4, C5, C6, C7	20pF/250V	6
C16, C17, C18, C19, C20	10 uF/100V	5
R3	50 $\Omega$	1
R1、R2	10 $\Omega$	2

### 10\*6 Plastic Package



Notes:

1. All dimensions are in mm;
2. The tolerances unless specified are  $\pm 0.2\text{mm}$ .



## Revision history

Table 4. Document revision history

Date	Revision	Datasheet Status
2024/6/27	V1.0	Preliminary Datasheet Creation

Application data based on: ZBB-24-17

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